

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4020B

MSI

14-stage binary counter

Product specification
File under Integrated Circuits, IC04

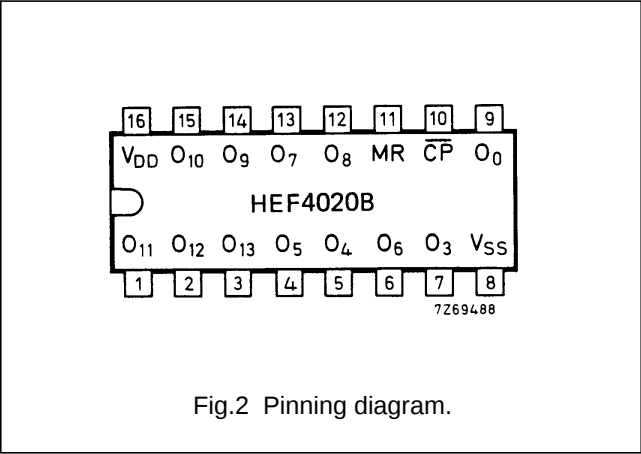
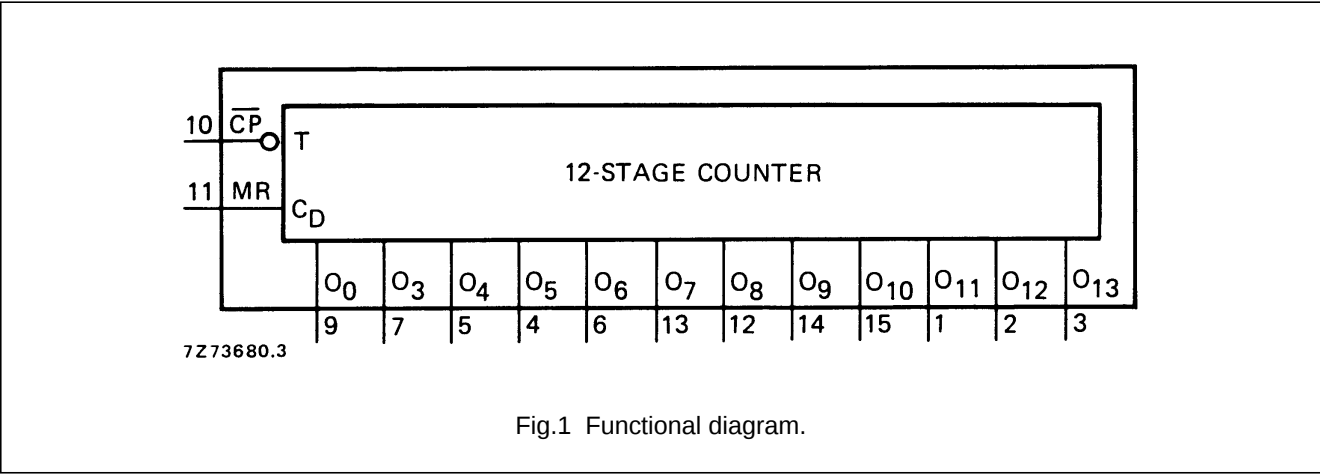
January 1995

14-stage binary counter

HEF4020B
MSI

DESCRIPTION

The HEF4020B is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0 , O_3 to O_{13}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. A feature of the HEF4020B is: high speed (typ. 35 MHz at $V_{DD} = 15\text{ V}$).



- HEF4020BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4020BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4020BT(D): 16-lead SO; plastic (SOT109-1)
(): Package Designator North America

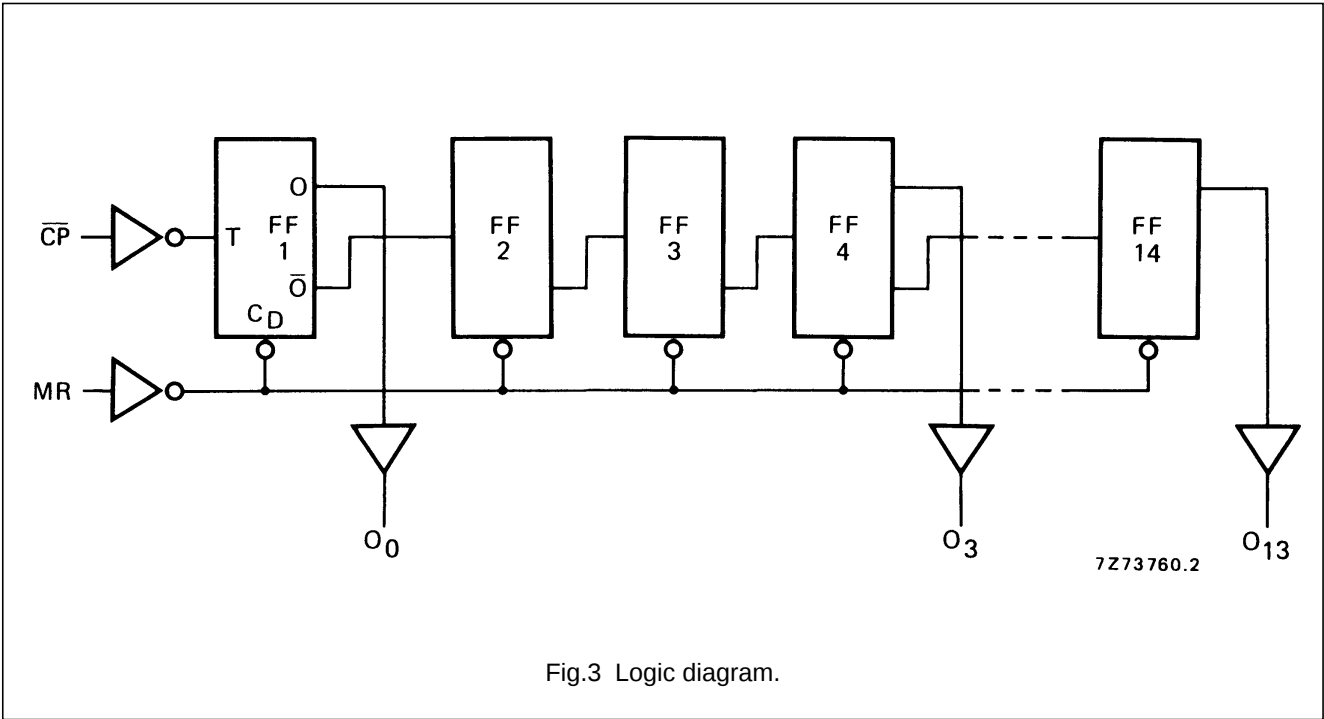
PINNING

- $\overline{CP}$ clock input (HIGH to LOW edge triggered)
MR master reset input (active HIGH)
 O_0 , O_3 to O_{13} parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI
See Family Specifications

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AC CHARACTERISTICS

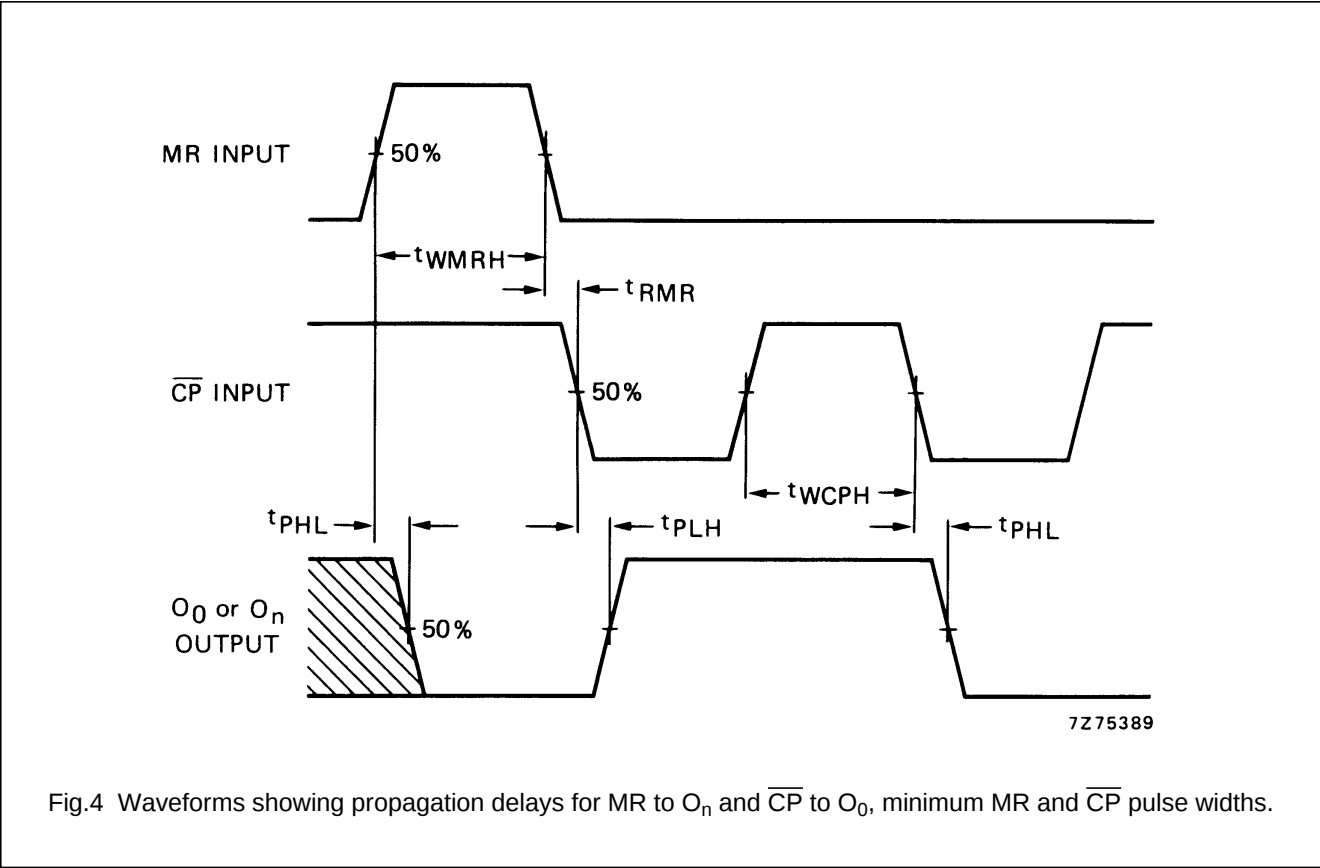
 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns; see also waveforms Fig.4

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $\overline{CP} \rightarrow O_0$ HIGH to LOW	5 10 15	t _{PHL}		105 45 30	210 90 65 ns	78 ns + (0,55 ns/pF) C _L 34 ns + (0,23 ns/pF) C _L 22 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5 10 15		t _{PLH}		105 50 35	210 95 70 ns	78 ns + (0,55 ns/pF) C _L 39 ns + (0,23 ns/pF) C _L 27 ns + (0,16 ns/pF) C _L
O _n → O _n + 1 HIGH to LOW	5 10 15			t _{PHL}		80 30 20	160 60 40 ns
LOW to HIGH	5 10 15	t _{PLH}				70 25 20	140 50 40 ns
MR → O _n HIGH to LOW	5 10 15		t _{PHL}			180 90 70	360 180 140 ns
Output transition times HIGH to LOW	5 10 15			t _{THL}		60 30 20	120 60 40 ns
LOW to HIGH	5 10 15	t _{TLH}				60 30 20	120 60 40 ns
Minimum clock pulse width; HIGH	5 10 15		t _{WCPH}		50 25 20	25 15 10	ns ns ns
Minimum MR pulse width; HIGH	5 10 15			t _{WMRH}	130 95 90	65 50 45	ns ns ns
Recovery time for MR	5 10 15	t _{RMR}			115 65 55	60 35 25	ns ns ns
Maximum clock pulse frequency	5 10 15		f _{max}		5 13 18	10 25 35	MHz MHz MHz

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	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$600 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$8\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$	



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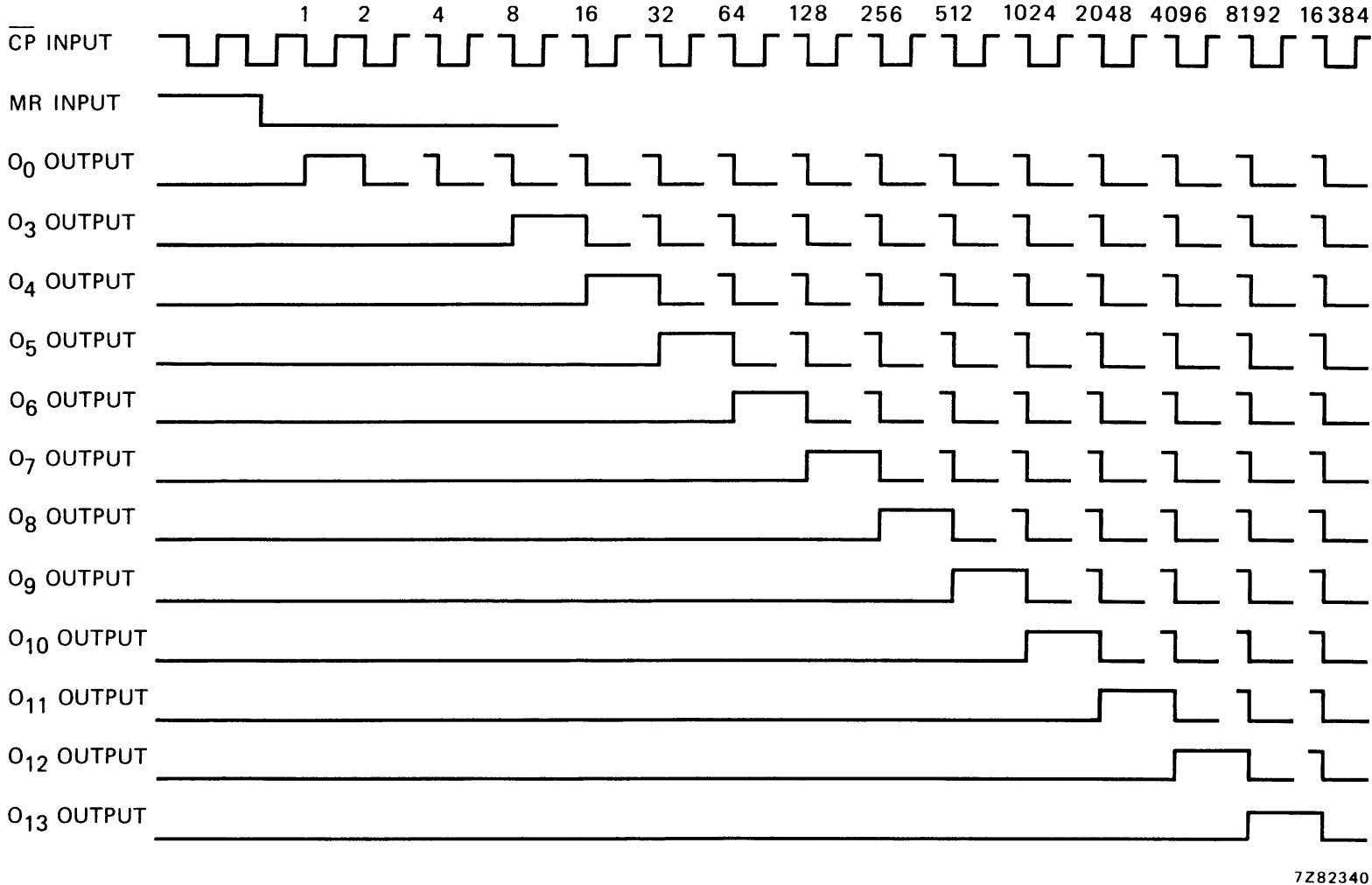


Fig.5 Timing diagram.