

FEATURES

- Timing From Microseconds to Hours
- Adjustable Duty Cycle
- Astable or Monostable Operation
- TTL-Compatible Output Can Sink or Source up to 200 mA

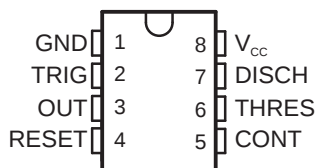
DESCRIPTION/ORDERING INFORMATION

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

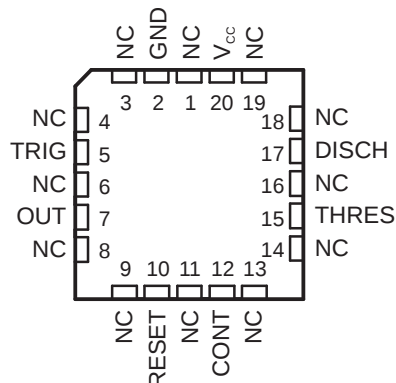
The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)



SE555...FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NA555, NE555, SA555, SE555 PRECISION TIMERS

SLFS022F – SEPTEMBER 1973 – REVISED JUNE 2006

ORDERING INFORMATION

T_A	$V_{THRES MAX}$ $V_{CC} = 15 V$	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	11.2 V	PDIP – P	Tube of 50	NE555P	NE555P
		SOIC – D	Tube of 75	NE555D	NE555
			Reel of 2500	NE555DR	
		SOP – PS	Reel of 2000	NE555PSR	N555
		TSSOP – PW	Tube of 150	NE555PW	N555
			Reel of 2000	NE555PWR	
–40°C to 85°C	11.2 V	PDIP – P	Tube of 50	SA555P	SA555P
		SOIC – D	Tube of 75	SA555D	SA555
			Reel of 2000	SA555DR	
–40°C to 105°C	11.2 V	PDIP – P	Tube of 50	NA555P	NA555P
		SOIC – D	Tube of 75	NA555D	NA555
			Reel of 2000	NA555DR	
–55°C to 125°C	10.6	PDIP – P	Tube of 50	SE555P	SE555P
		SOIC – D	Tube of 75	SE555D	SE555D
			Reel of 2500	SE555DR	
		CDIP – JG	Tube of 50	SE555JG	SE555JG
		LCCC – FK	Tube of 55	SE555FK	SE555FK

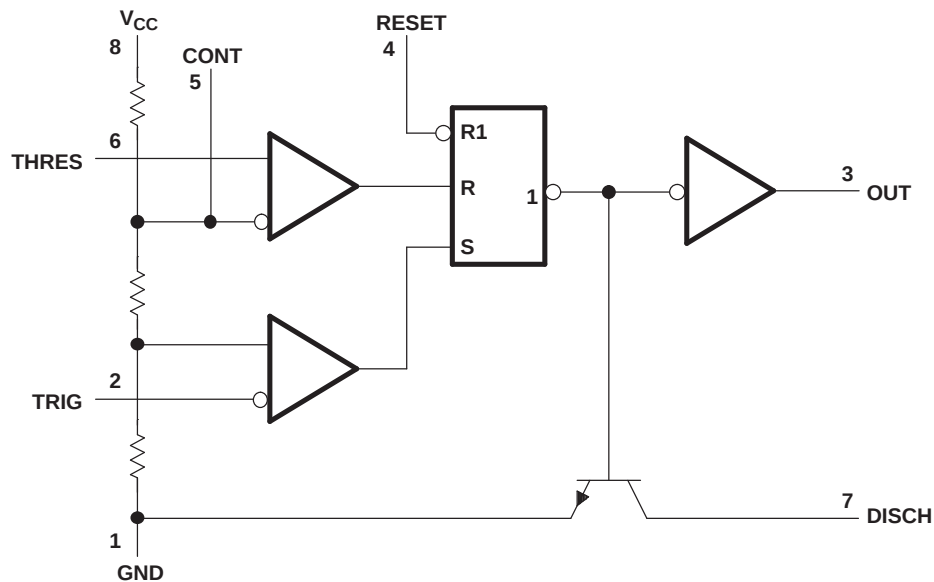
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE ⁽¹⁾	THRESHOLD VOLTAGE ⁽¹⁾	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	$< 1/3 V_{DD}$	Irrelevant	High	Off
High	$> 1/3 V_{DD}$	$> 2/3 V_{DD}$	Low	On
High	$> 1/3 V_{DD}$	$< 2/3 V_{DD}$	As previously established	

(1) Voltage levels shown are nominal.

FUNCTIONAL BLOCK DIAGRAM



Pin numbers shown are for the D, JG, P, PS, and PW packages.
 NOTE A: RESET can override TRIG, which can override THRES.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾			18	V
V_I	Input voltage	CONT, RESET, THRES, TRIG		V_{CC}	V
I_O	Output current			± 225	mA
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package		97	$^{\circ}\text{C/W}$
		P package		85	
		PS package		95	
		PW package		149	
θ_{JC}	Package thermal impedance ⁽⁵⁾⁽⁶⁾	FK package		5.61	$^{\circ}\text{C/W}$
		JG package		14.5	
T_J	Operating virtual junction temperature			150	$^{\circ}\text{C}$
	Case temperature for 60 s	FK package		260	$^{\circ}\text{C}$
	Lead temperature 1, 6 mm (1/16 in) from case for 60 s	JG package		300	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		–65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(\text{max}) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with MIL-STD-883.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	NA555, NE555, SA555	4.5	16	V
		SE555	4.5	18	
V_I	Input voltage	CONT, RESET, THRES, and TRIG		V_{CC}	V
I_O	Output current			± 200	mA
T_A	Operating free-air temperature	NA555	–40	105	$^{\circ}\text{C}$
		NE555	0	70	
		SA555	–40	85	
		SE555	–55	125	

Electrical Characteristics

$V_{CC} = 5\text{ V}$ to 15 V , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	V _{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V _{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
THRES current ⁽¹⁾			30	250		30	250		nA
TRIG voltage level	V _{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
		T _A = −55°C to 125°C	3		6				
	V _{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
		T _A = −55°C to 125°C			1.9				
TRIG current	TRIG at 0 V		0.5	0.9		0.5	2		μA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	T _A = −55°C to 125°C				1.1				
RESET current	RESET at V _{CC}		0.1	0.4		0.1	0.4		mA
	RESET at 0 V		−0.4	−1		−0.4	−1.5		
DISCH switch off-state current			20	100		20	100		nA
CONT voltage (open circuit)	V _{CC} = 15 V		9.6	10	10.4	9	10	11	V
		T _A = −55°C to 125°C	9.6		10.4				
	V _{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
		T _A = −55°C to 125°C	2.9		3.8				
Low-level output voltage	V _{CC} = 15 V, I _{OL} = 10 mA		0.1	0.15		0.1	0.25	V	
		T _A = −55°C to 125°C			0.2				
	V _{CC} = 15 V, I _{OL} = 50 mA		0.4	0.5		0.4	0.75		
		T _A = −55°C to 125°C			1				
	V _{CC} = 15 V, I _{OL} = 100 mA		2	2.2		2	2.5		
		T _A = −55°C to 125°C			2.7				
	V _{CC} = 15 V, I _{OL} = 200 mA		2.5			2.5			
	V _{CC} = 5 V, I _{OL} = 3.5 mA	T _A = −55°C to 125°C			0.35				
V _{CC} = 5 V, I _{OL} = 5 mA		0.1	0.2		0.1	0.35			
	T _A = −55°C to 125°C			0.8					
V _{CC} = 5 V, I _{OL} = 8 mA		0.15	0.25		0.15	0.4			
High-level output voltage	V _{CC} = 15 V, I _{OL} = −100 mA		13	13.3		12.75	13.3	V	
		T _A = −55°C to 125°C	12						
	V _{CC} = 15 V, I _{OH} = −200 mA		12.5			12.5			
	V _{CC} = 15 V, I _{OL} = −100 mA		3	3.3		2.75	3.3		
		T _A = −55°C to 125°C	2						
Supply current	Output low, No load	V _{CC} = 15 V	10	12		10	15	mA	
		V _{CC} = 5 V	3	5		3	6		
	Output high, No load	V _{CC} = 15 V	9	10		9	13		
		V _{CC} = 5 V	2	4		2	5		

(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of [Figure 12](#). For example, when $V_{CC} = 5\text{ V}$, the maximum value is $R = R_A + R_B \approx 3.4\text{ M}\Omega$, and for $V_{CC} = 15\text{ V}$, the maximum value is $10\text{ M}\Omega$.

Operating Characteristics

$V_{CC} = 5\text{ V to }15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval ⁽²⁾	Each timer, monostable ⁽³⁾	$T_A = 25^\circ\text{C}$		0.5	1.5 ⁽⁴⁾		1	3	%
	Each timer, astable ⁽⁵⁾			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable ⁽³⁾	$T_A = \text{MIN to MAX}$		30	100 ⁽⁴⁾		50		ppm/ °C
	Each timer, astable ⁽⁵⁾			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable ⁽³⁾	$T_A = 25^\circ\text{C}$		0.05	0.2 ⁽⁴⁾		0.1	0.5	%/V
	Each timer, astable ⁽⁵⁾			0.15			0.3		
Output-pulse rise time		$C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$		100	200 ⁽⁴⁾		100	300	ns
Output-pulse fall time		$C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$		100	200 ⁽⁴⁾		100	300	ns

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
- (2) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
- (3) Values specified are for a device in a monostable circuit similar to [Figure 9](#), with the following component values: $R_A = 2\text{ k}\Omega$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$.
- (4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (5) Values specified are for a device in an astable circuit similar to [Figure 12](#), with the following component values: $R_A = 1\text{ k}\Omega$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$.

TYPICAL CHARACTERISTICS

Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

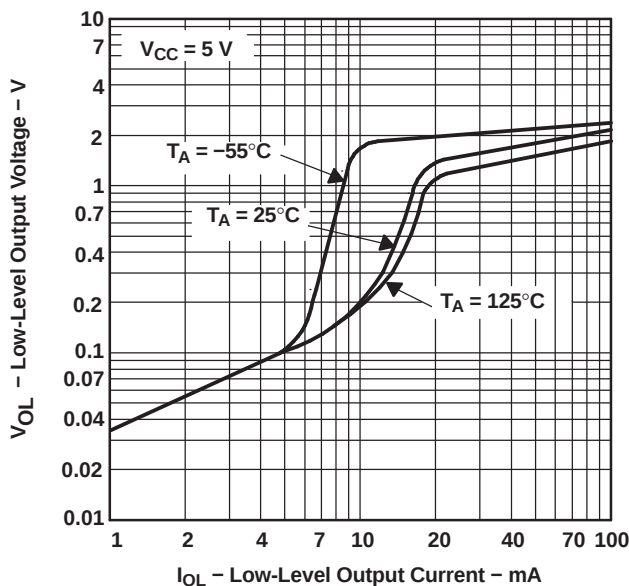


Figure 1.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

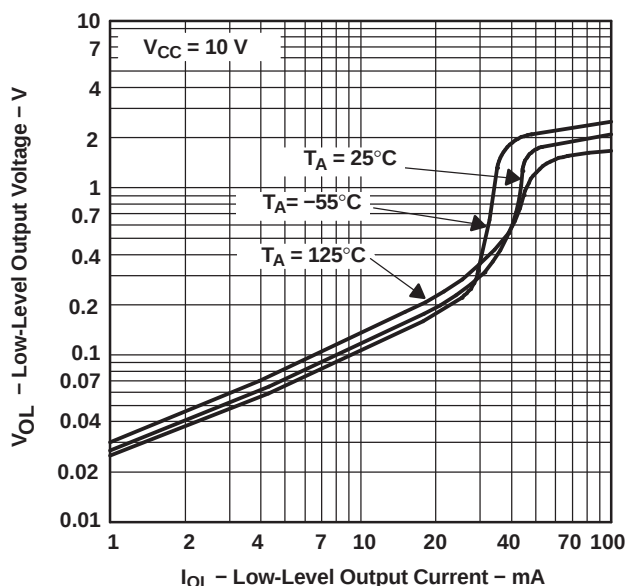


Figure 2.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

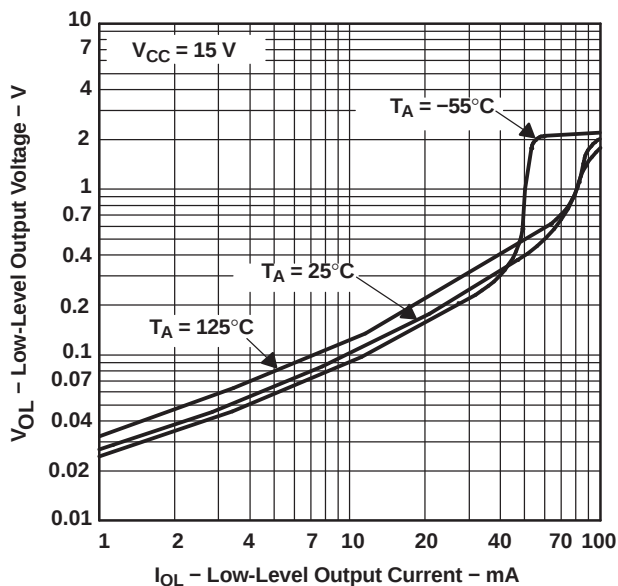


Figure 3.

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

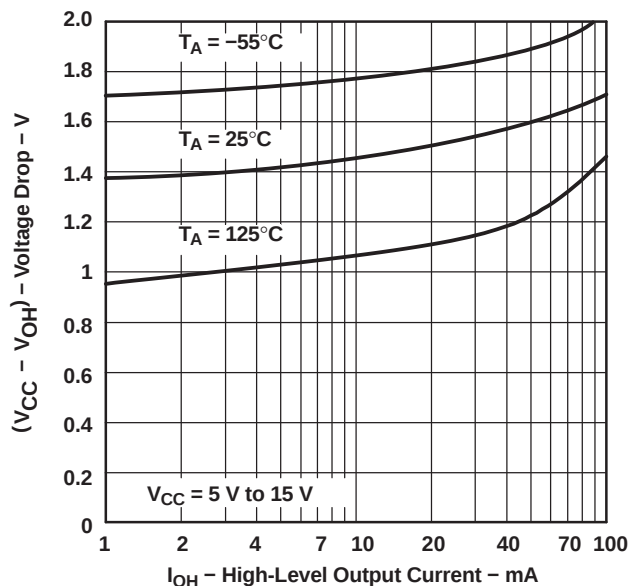


Figure 4.

TYPICAL CHARACTERISTICS (continued)

Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

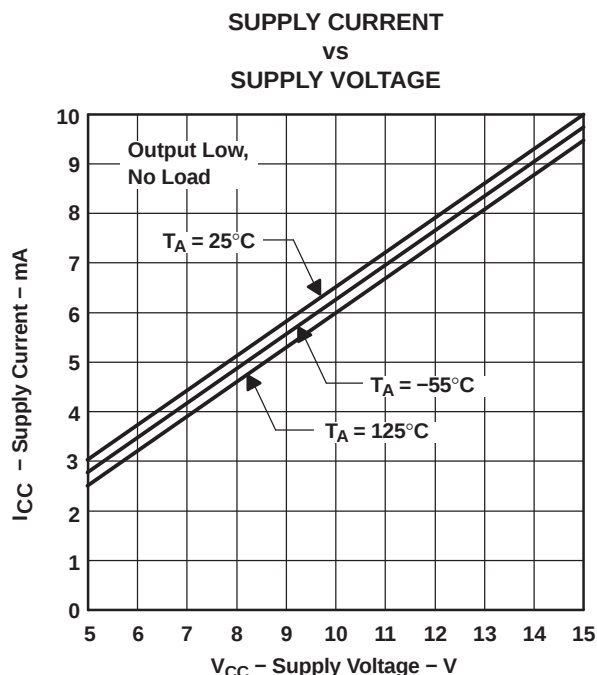


Figure 5.

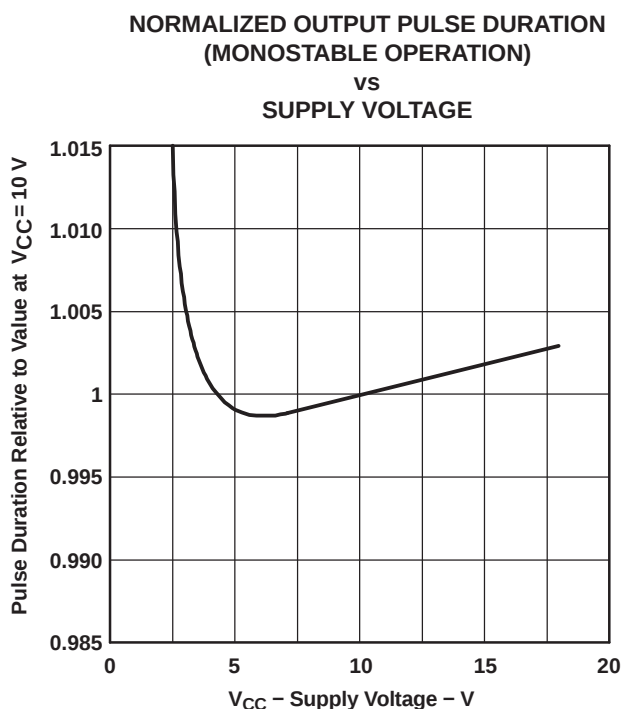


Figure 6.

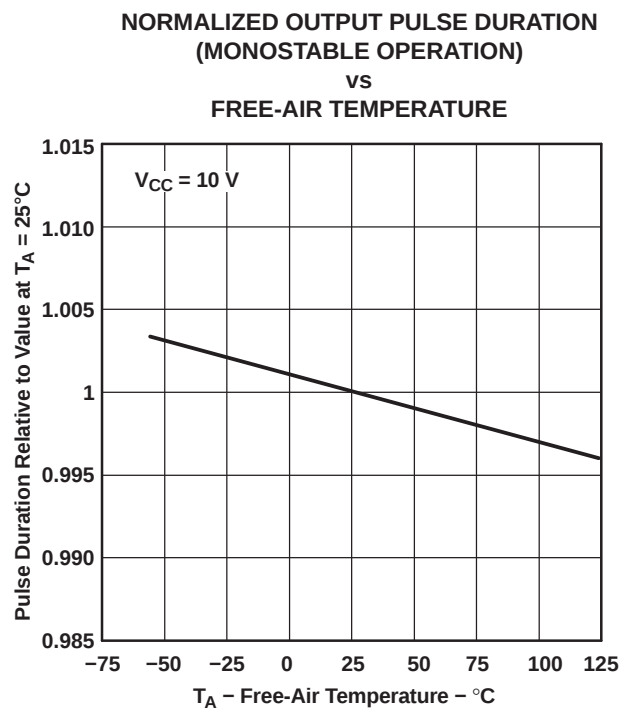


Figure 7.

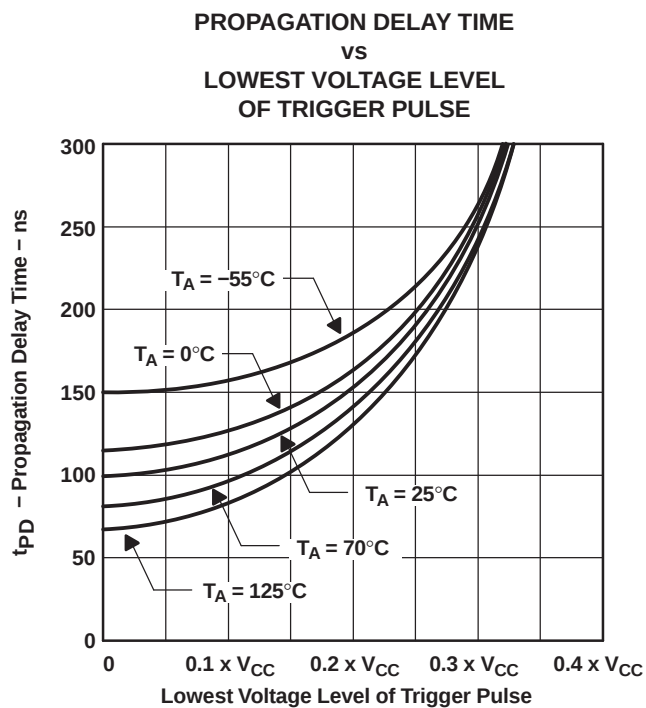
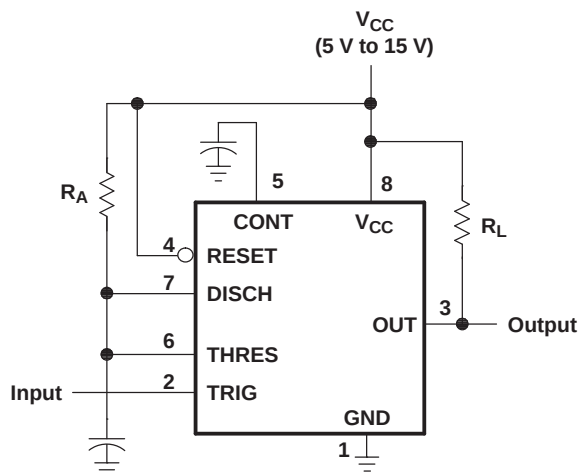


Figure 8.

APPLICATION INFORMATION

Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC} . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC} .

APPLICATION INFORMATION (continued)

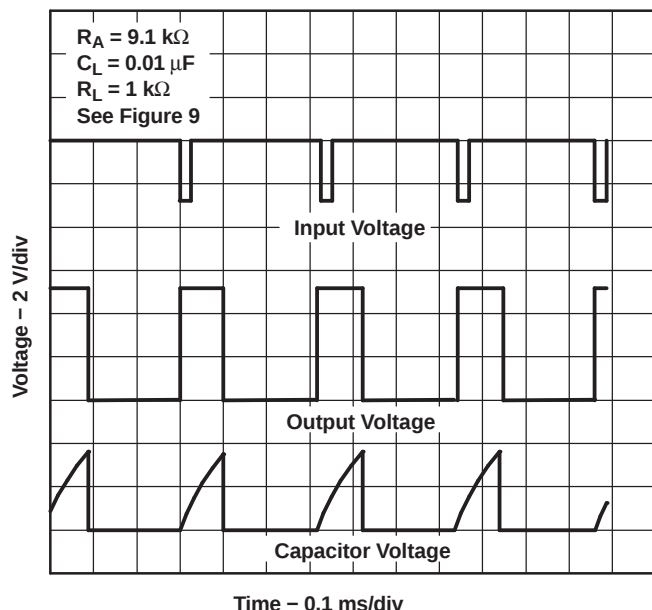


Figure 10. Typical Monostable Waveforms

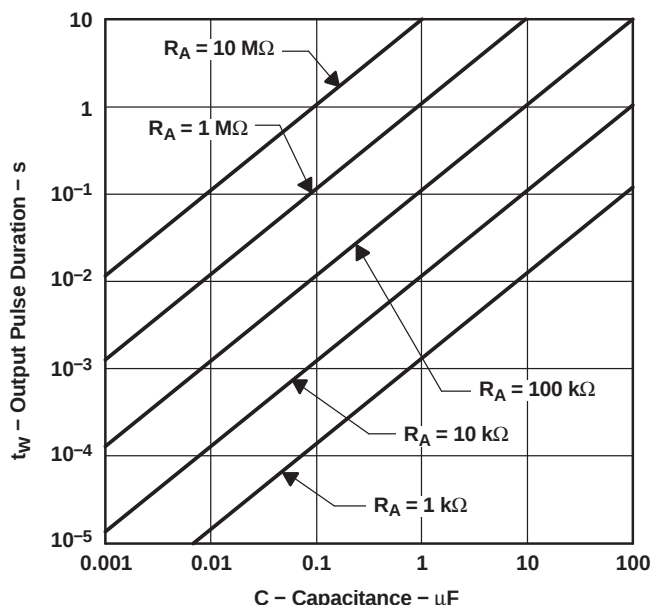
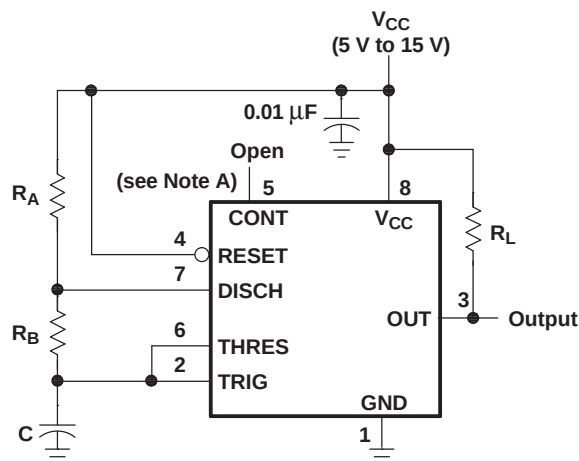


Figure 11. Output Pulse Duration vs Capacitance

Astable Operation

As shown in Figure 12, adding a second resistor, R_B , to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

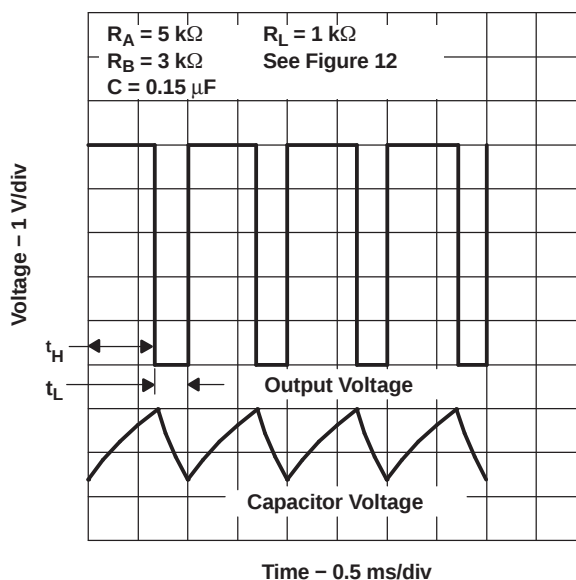


Figure 13. Typical Astable Waveforms

APPLICATION INFORMATION (continued)

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693 (R_A + R_B) C$$

$$t_L = 0.693 (R_B) C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693 (R_A + 2R_B) C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B) C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\begin{aligned} \text{Output waveform duty cycle} \\ = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \end{aligned}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

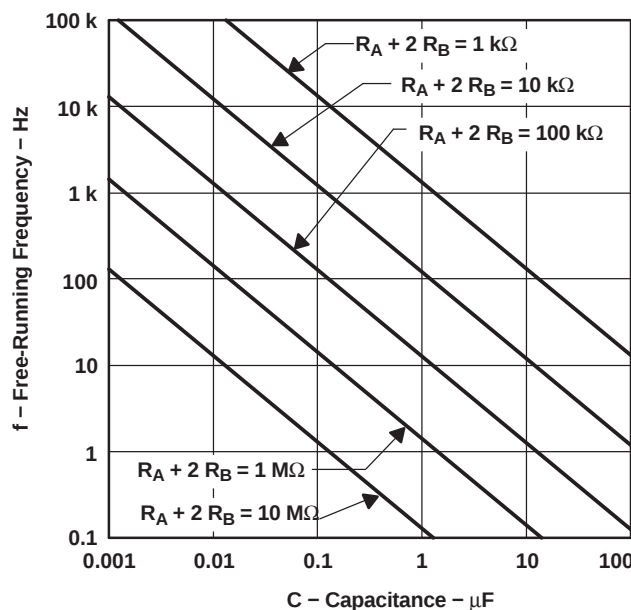
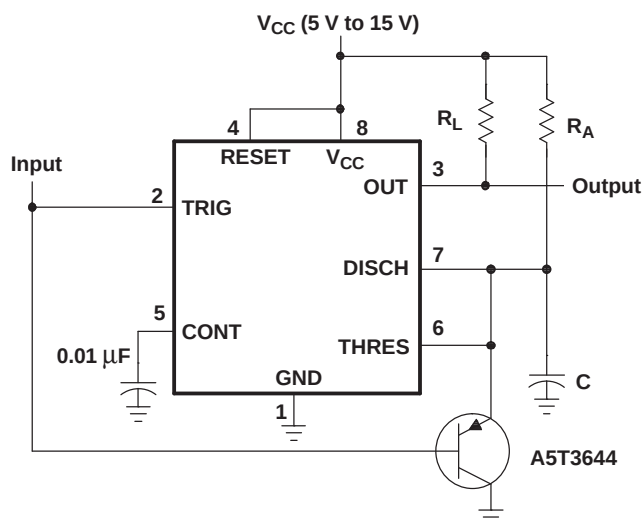


Figure 14. Free-Running Frequency

Missing-Pulse Detector

The circuit shown in Figure 15 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 16.



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 15. Circuit for Missing-Pulse Detector

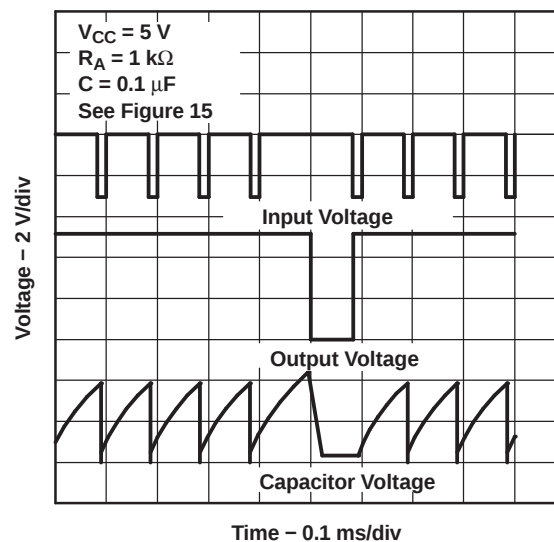


Figure 16. Completed Timing Waveforms for Missing-Pulse Detector

APPLICATION INFORMATION (continued)

Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of [Figure 9](#) can be made to operate as a frequency divider. [Figure 17](#) shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

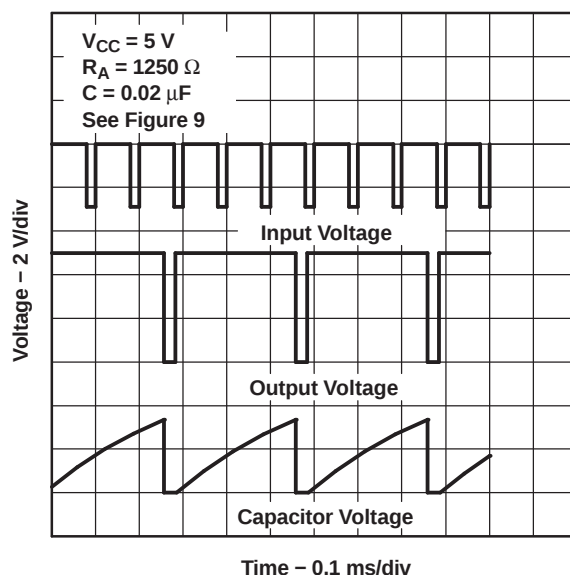
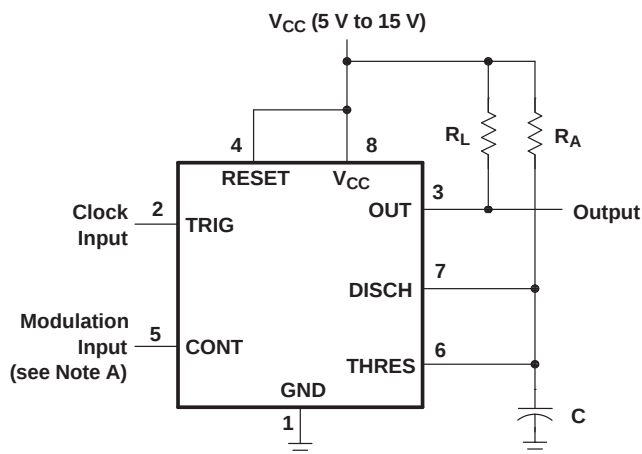


Figure 17. Divide-by-Three Circuit Waveforms

APPLICATION INFORMATION (continued)

Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

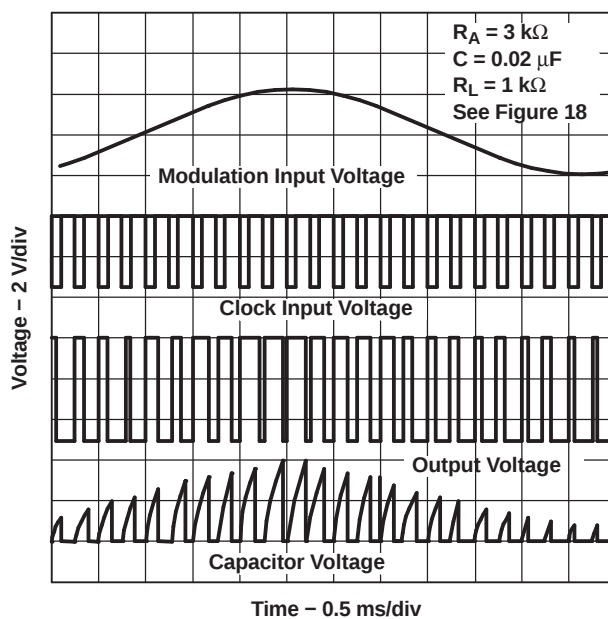
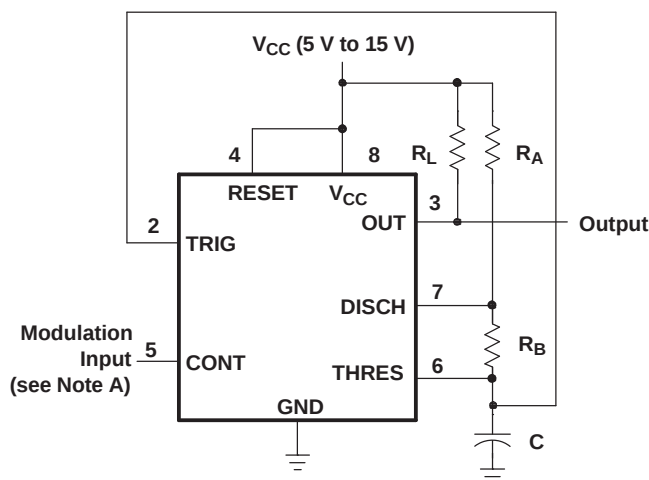


Figure 19. Pulse-Width-Modulation Waveforms

APPLICATION INFORMATION (continued)

Pulse-Position Modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

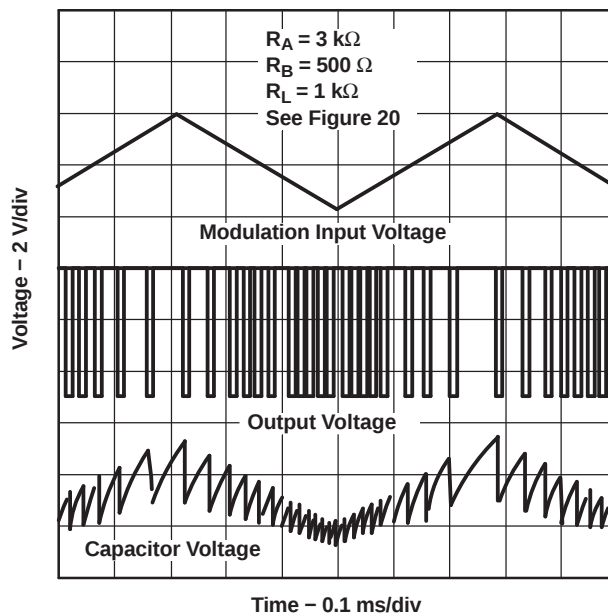
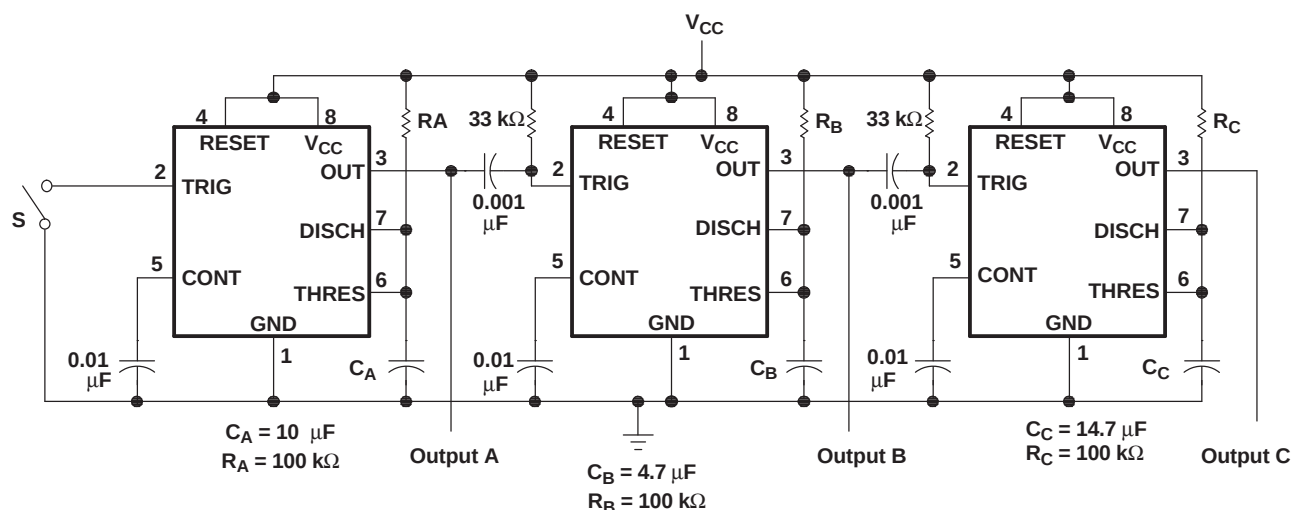


Figure 21. Pulse-Position-Modulation Waveforms

APPLICATION INFORMATION (continued)

Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. [Figure 22](#) shows a sequencer circuit with possible applications in many systems, and [Figure 23](#) shows the output waveforms.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: S closes momentarily at $t = 0$.

Figure 22. Sequential Timer Circuit

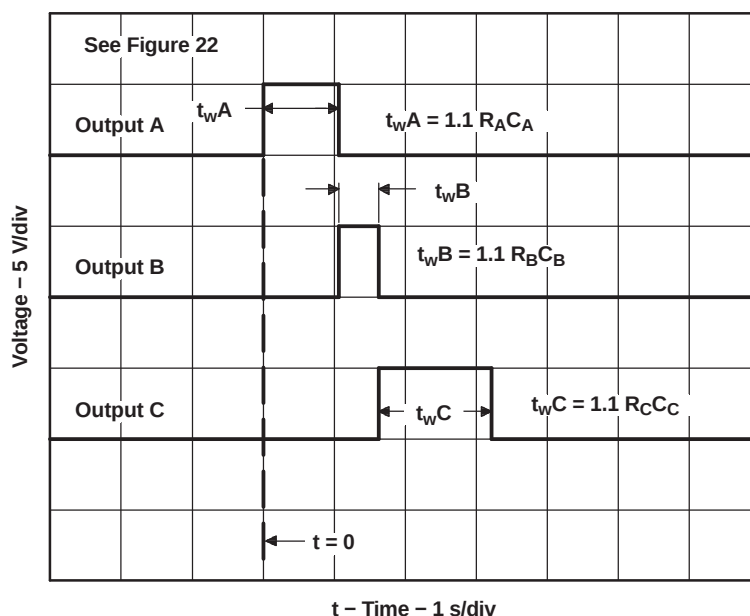


Figure 23. Sequential Timer Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/10901BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
NA555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NA555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE555PSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI
NE555PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555Y	OBSOLETE			0		TBD	Call TI	Call TI

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SA555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SA555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SE555D	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
SE555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SE555DR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
SE555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SE555FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SE555JG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
SE555JGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
SE555N	OBSOLETE	PDIP	N	8		TBD	Call TI	Call TI
SE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

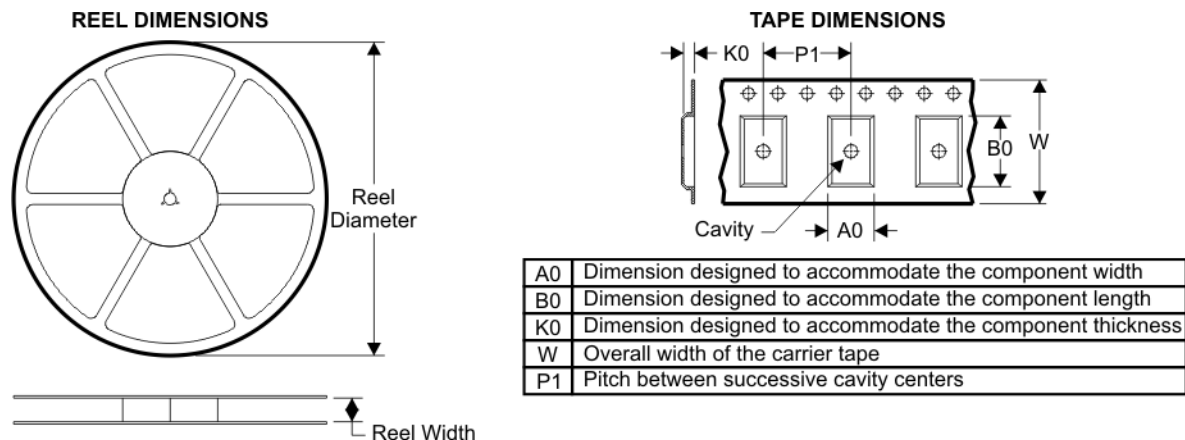
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the

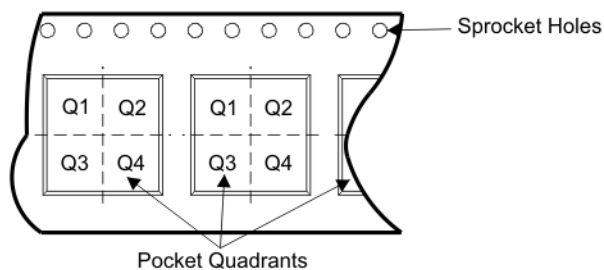
accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION

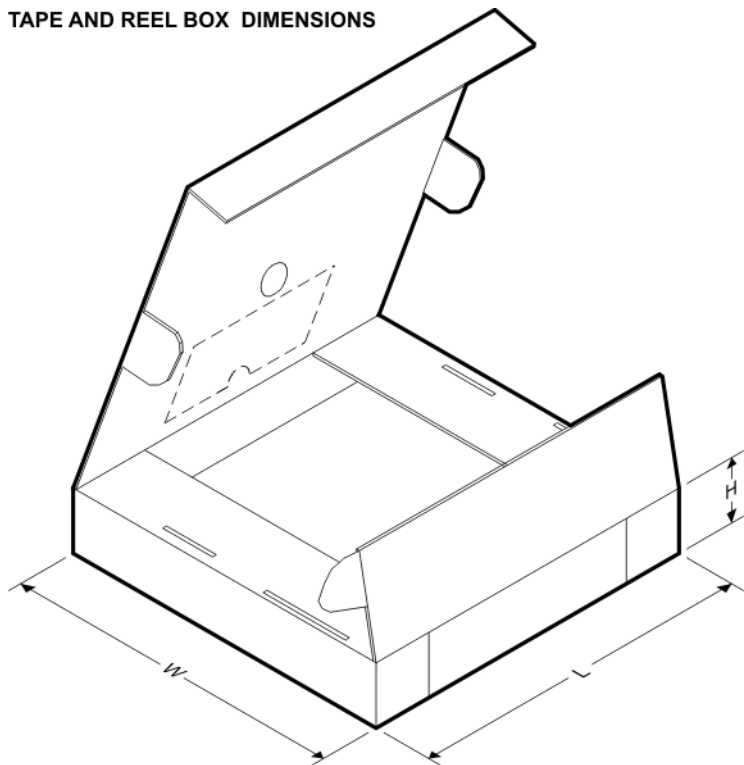


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NA555DR	D	8	SITE 27	330	12	6.4	5.2	2.1	8	12	Q1
NA555DR	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
NE555DR	D	8	SITE 27	330	12	6.4	5.2	2.1	8	12	Q1
NE555DR	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1
NE555PSR	PS	8	SITE 41	330	16	8.2	6.6	2.5	12	16	Q1
NE555PWR	PW	8	SITE 41	330	12	7.0	3.6	1.6	8	12	Q1
SA555DR	D	8	SITE 27	330	12	6.4	5.2	2.1	8	12	Q1

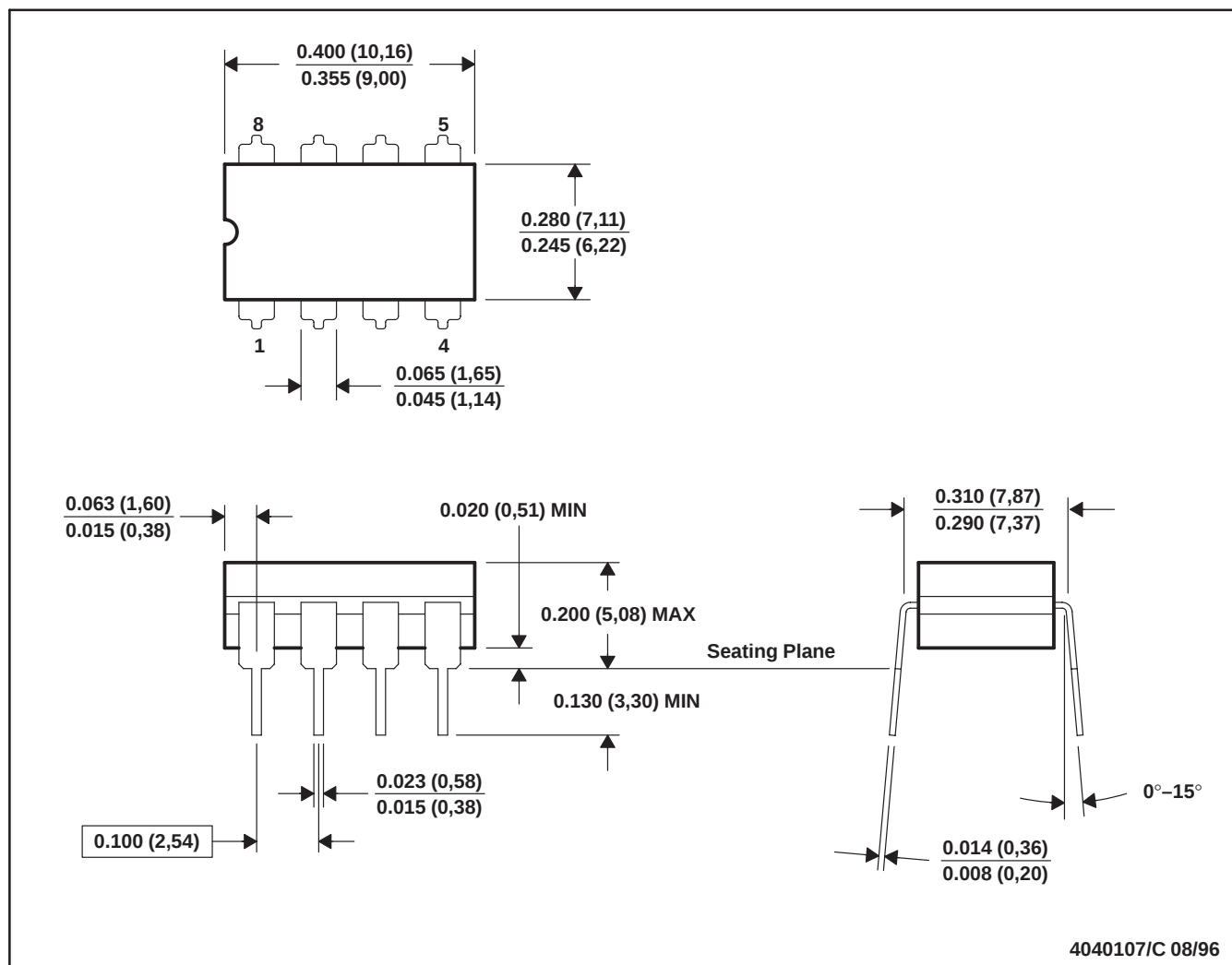
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
NA555DR	D	8	SITE 27	342.9	336.6	20.64
NA555DR	D	8	SITE 41	346.0	346.0	29.0
NE555DR	D	8	SITE 27	342.9	336.6	20.64
NE555DR	D	8	SITE 41	346.0	346.0	29.0
NE555PSR	PS	8	SITE 41	346.0	346.0	33.0
NE555PWR	PW	8	SITE 41	346.0	346.0	29.0
SA555DR	D	8	SITE 27	342.9	336.6	20.64

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

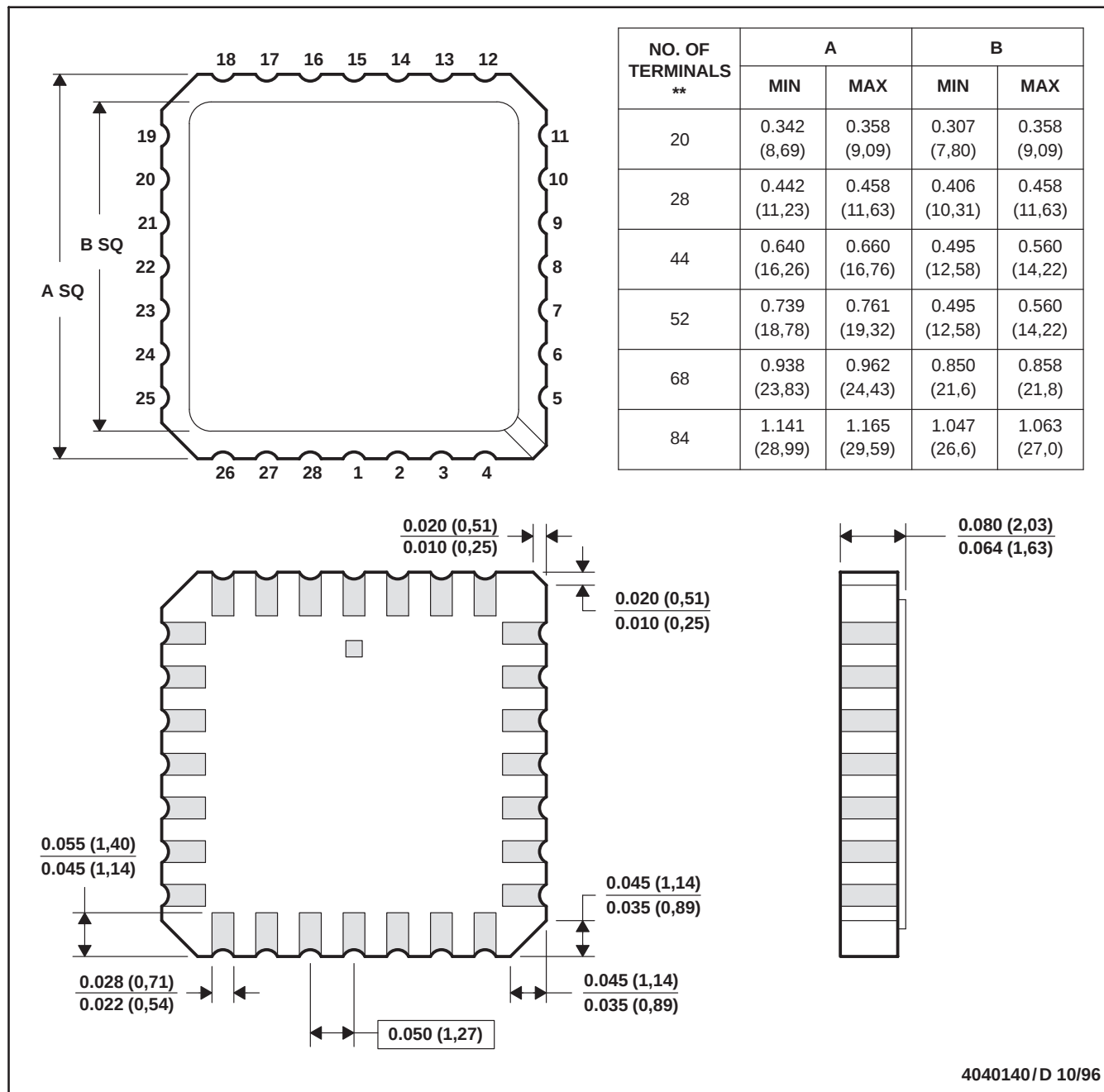


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification.
 - Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

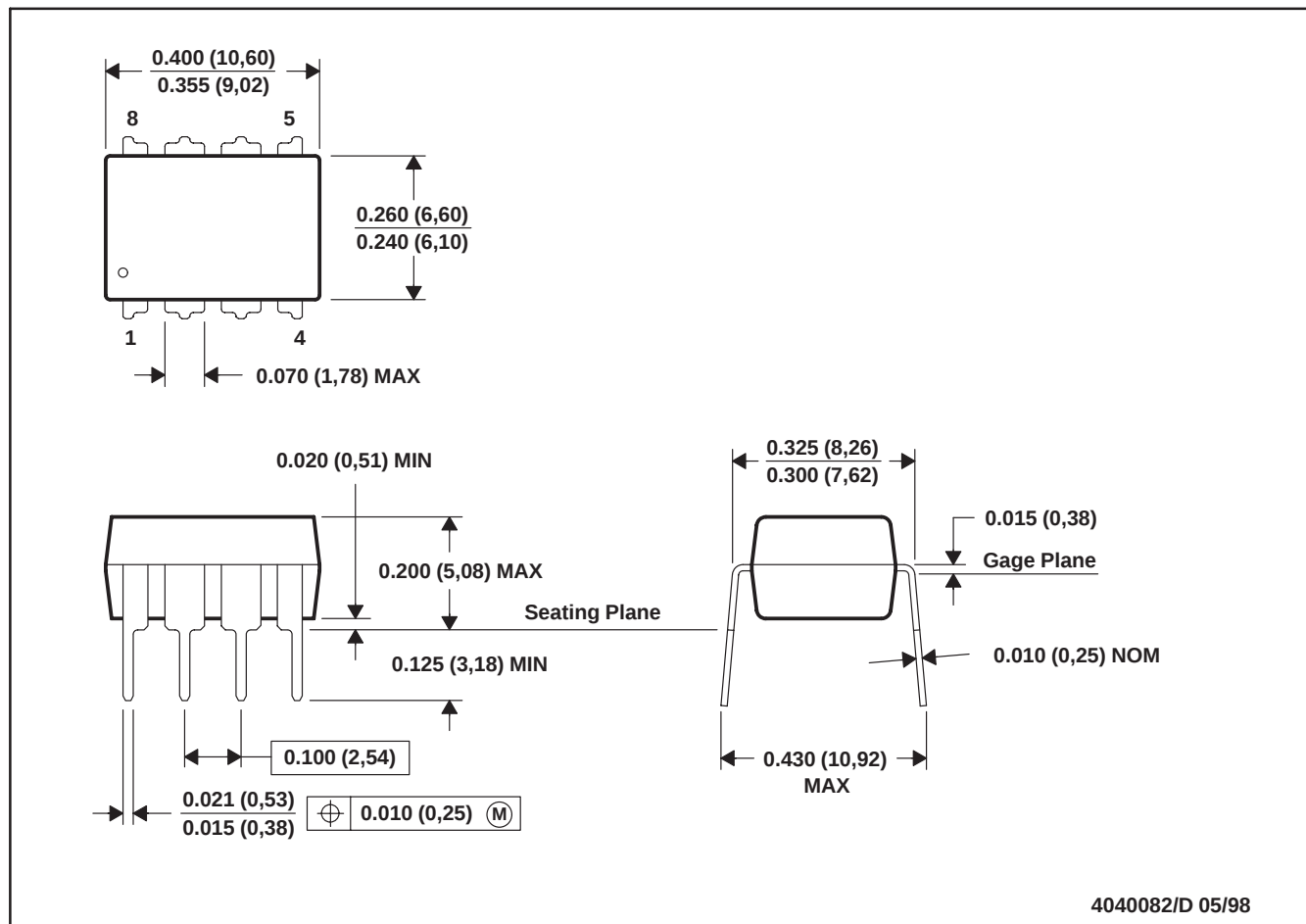
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

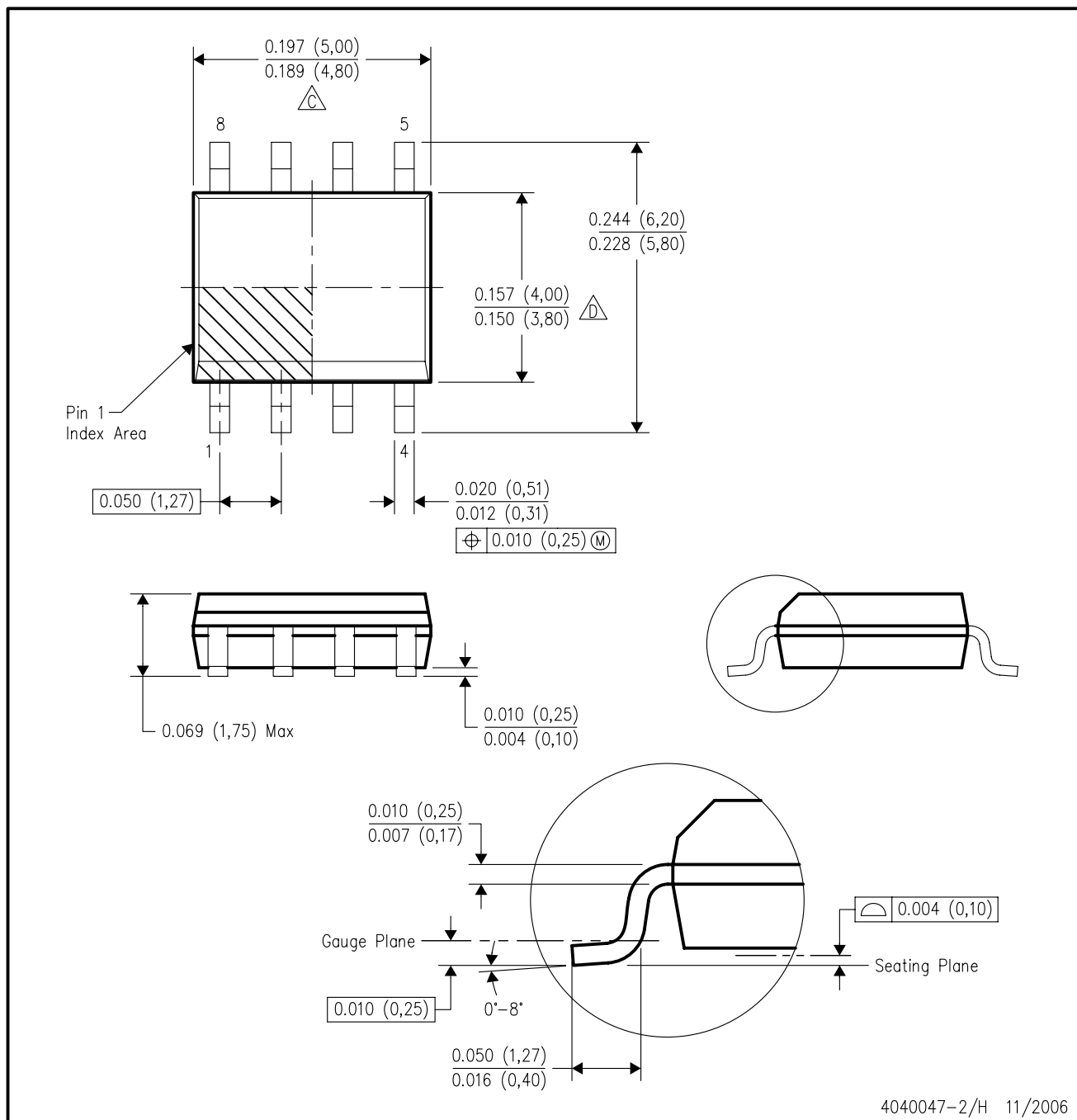


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

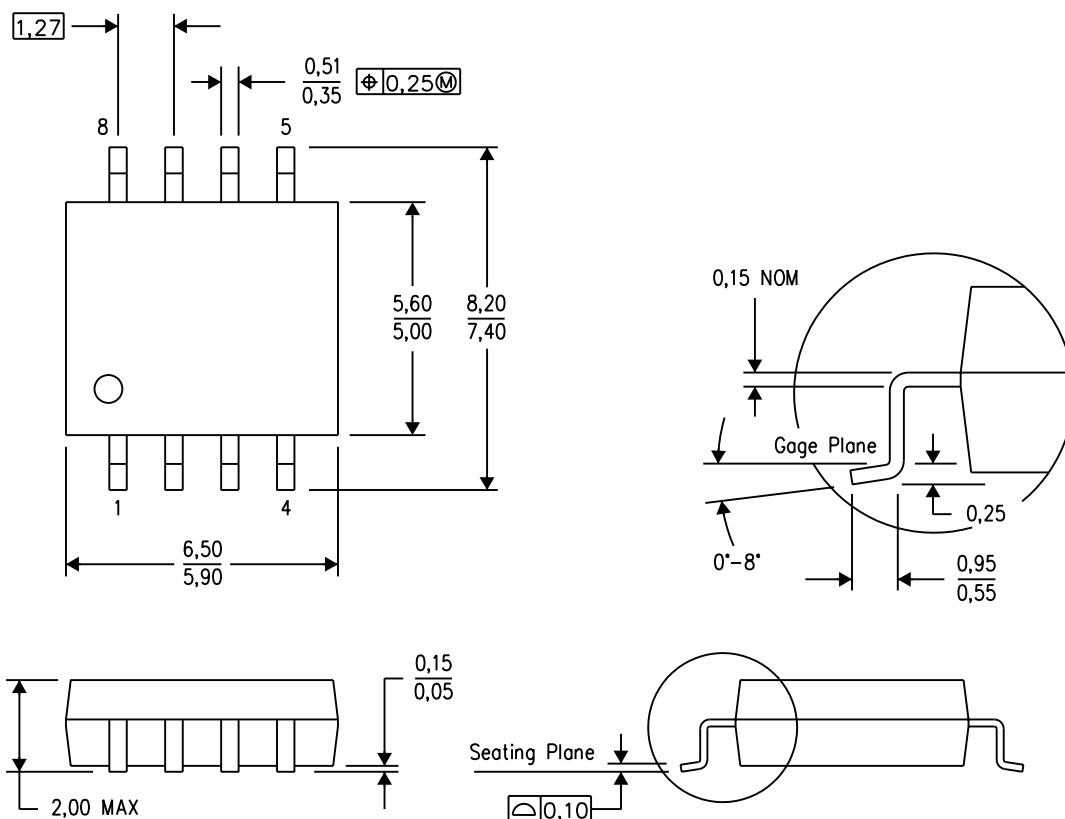


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



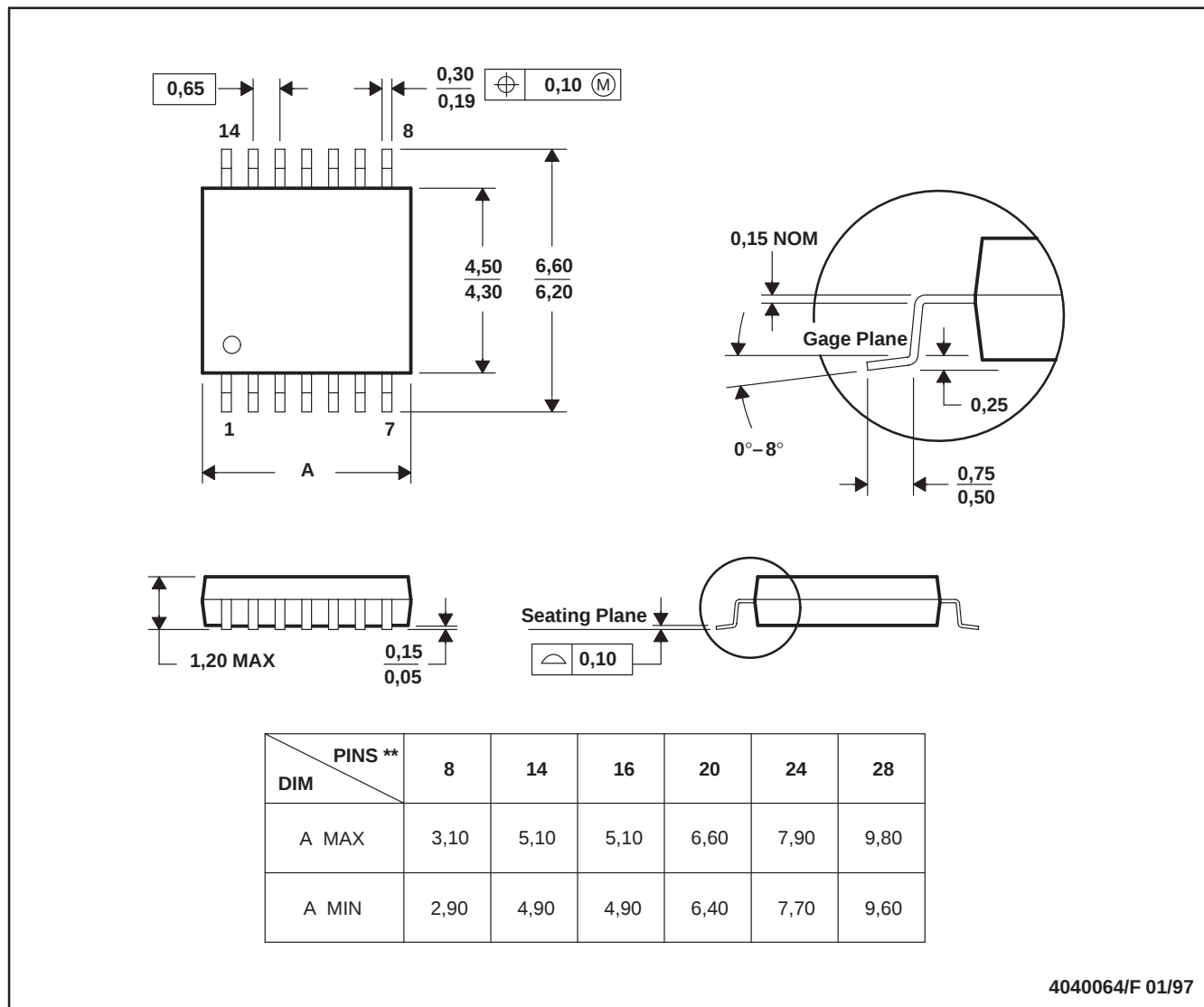
4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated