

# I<sup>2</sup>C CONTROLLED KEYPAD SCAN IC WITH INTEGRATED ESD PROTECTION

## FEATURES

- Operating Power-Supply Voltage Range of 1.65 V to 3.6 V
- Supports QWERTY Keypad Operation Plus GPIO Expansion
- 18 GPIOs Can Be Configured into Eight Inputs and Ten Outputs to Support an 8 × 10 Keypad Array (80 Buttons)
- ESD Protection Exceeds JESD 22 on all 18 GPIO Pins and non GPIO pins
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged Device Model (C101)
- Low Standby (Idle) Current Consumption: 3 µA
- Polling Current Drain 70 µA for One Key Pressed
- 10 Byte FIFO to Store 10 Key Presses and Releases
- Supports 1-MHz Fast Mode Plus I<sup>2</sup>C Bus
- Open-Drain Active-Low Interrupt Output, Asserted when Key is Pressed and Key is Released
- Minimum Debounce Time of 50 µs
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the SCL and SDA Inputs: Typical V<sub>hys</sub> at 1.8 V is 0.18 V
- Latch-Up Performance Exceeds 200 mA Per JESD 78, Class II
- Very Small Packages
  - WCSP (YFP): 2 mm × 2 mm; 0.4 mm pitch
  - QFN (RTW): 4 mm × 4 mm; 0.5 mm pitch

## APPLICATIONS

- Smart Phones
- PDAs
- GPS Devices
- MP3 Players
- Digital Cameras

## DESCRIPTION/ORDERING INFORMATION

The TCA8418 is a keypad scan device with integrated ESD protection. It can operate from 1.65 V to 3.6 V and has 18 general purpose inputs/outputs (GPIO) that can be used to support up to 80 keys via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

The key controller includes an oscillator that debounces at 50 µs and maintains a 10 byte FIFO of key-press and release events which can store up to 10 keys with overflow wrap capability. An interrupt (/INT) output can be configured to alert key presses and releases either as they occur, or at maximum rate. Also, for the YFP package, a CAD\_INT pin is included to indicate the detection of CTRL-ALT-DEL (i.e., 1, 11, 21) key press action.

The major benefit of this device is it frees up the processor from having to scan the keypad for presses and releases. This provides power and bandwidth savings. The TCA8418 is also ideal for usage with processors that have limited GPIOs.

## ORDERING INFORMATION

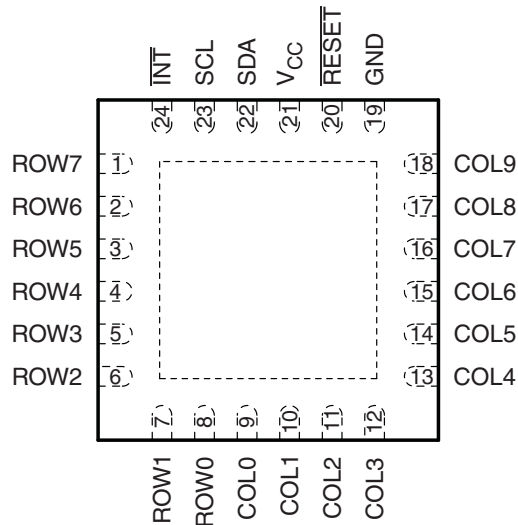
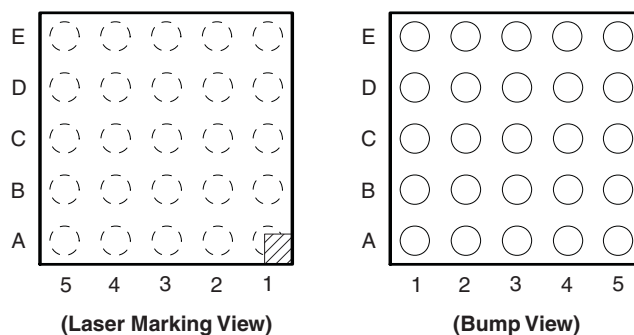
| T <sub>A</sub> | PACKAGE <sup>(1)(2)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RTW                 | Tape and reel | TCA8418RTWR           | PZ418            |
|                | WCSP – YFP                | Tape and reel | TCA8418YFPR           | PREVIEW          |

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**RTW PACKAGE  
(TOP VIEW)**

**YFP PACKAGE**

**YFP Package Terminal Assignments**

|          |                           |          |          |                              |          |
|----------|---------------------------|----------|----------|------------------------------|----------|
| <b>E</b> | $\overline{\text{INT}}$   | GND      | COL5     | COL0                         | ROW3     |
| <b>D</b> | SCL                       | COL9     | COL4     | ROW0                         | ROW4     |
| <b>C</b> | SDA                       | COL8     | COL3     | ROW1                         | ROW5     |
| <b>B</b> | $V_{CC}$                  | COL7     | COL2     | $\overline{\text{CAD\_INT}}$ | ROW6     |
| <b>A</b> | $\overline{\text{RESET}}$ | COL6     | COL1     | ROW2                         | ROW7     |
|          | <b>5</b>                  | <b>4</b> | <b>3</b> | <b>2</b>                     | <b>1</b> |

**TERMINAL FUNCTIONS**

| TERMINAL     |               |                              | TYPE | DESCRIPTION                                                                                                                                          |
|--------------|---------------|------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO.          |               | NAME                         |      |                                                                                                                                                      |
| QFN<br>(RTW) | WCSP<br>(YFP) |                              |      |                                                                                                                                                      |
| 1            | A1            | ROW7                         | I/O  | GPIO or row 7 in keypad matrix                                                                                                                       |
| 2            | B1            | ROW6                         | I/O  | GPIO or row 6 in keypad matrix                                                                                                                       |
| 3            | C1            | ROW5                         | I/O  | GPIO or row 5 in keypad matrix                                                                                                                       |
| 4            | D1            | ROW4                         | I/O  | GPIO or row 4 in keypad matrix                                                                                                                       |
| 5            | E1            | ROW3                         | I/O  | GPIO or row 3 in keypad matrix                                                                                                                       |
| 6            | A2            | ROW2                         | I/O  | GPIO or row 2 in keypad matrix                                                                                                                       |
| 7            | C2            | ROW1                         | I/O  | GPIO or row 1 in keypad matrix                                                                                                                       |
| 8            | D2            | ROW0                         | I/O  | GPIO or row 0 in keypad matrix                                                                                                                       |
| 9            | E2            | COL0                         | I/O  | GPIO or column 0 in keypad matrix                                                                                                                    |
| 10           | A3            | COL1                         | I/O  | GPIO or column 1 in keypad matrix                                                                                                                    |
| 11           | B3            | COL2                         | I/O  | GPIO or column 2 in keypad matrix                                                                                                                    |
| 12           | C3            | COL3                         | I/O  | GPIO or column 3 in keypad matrix                                                                                                                    |
| 13           | D3            | COL4                         | I/O  | GPIO or column 4 in keypad matrix                                                                                                                    |
| 14           | E3            | COL5                         | I/O  | GPIO or column 5 in keypad matrix                                                                                                                    |
| 15           | A4            | COL6                         | I/O  | GPIO or column 6 in keypad matrix                                                                                                                    |
| 16           | B4            | COL7                         | I/O  | GPIO or column 7 in keypad matrix                                                                                                                    |
| 17           | C4            | COL8                         | I/O  | GPIO or column 8 in keypad matrix                                                                                                                    |
| 18           | D4            | COL9                         | I/O  | GPIO or column 9 in keypad matrix                                                                                                                    |
| 19           | E4            | GND                          | –    | Ground                                                                                                                                               |
| 20           | A5            | $\overline{\text{RESET}}$    | I    | Active-low reset input. Connect to V <sub>CC</sub> through a pullup resistor, if no active connection is used.                                       |
| 21           | B5            | V <sub>CC</sub>              | Pwr  | Supply voltage of 1.65 V to 3.6 V                                                                                                                    |
| 22           | C5            | SDA                          | I/O  | Serial data bus. Connect to V <sub>CC</sub> through a pullup resistor.                                                                               |
| 23           | D5            | SCL                          | I    | Serial clock bus. Connect to V <sub>CC</sub> through a pullup resistor.                                                                              |
| 24           | E5            | $\overline{\text{INT}}$      | O    | Active-low interrupt output. Open drain structure. Connect to V <sub>CC</sub> through a pullup resistor.                                             |
| –            | B2            | $\overline{\text{CAD\_INT}}$ | O    | Active-low interrupt hardware output for 3-key simultaneous press-event. Open drain structure. Connect to V <sub>CC</sub> through a pullup resistor. |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

|                  |                                                                                             |                         | MIN                                   | MAX | UNIT |
|------------------|---------------------------------------------------------------------------------------------|-------------------------|---------------------------------------|-----|------|
| V <sub>CC</sub>  | Supply voltage range                                                                        |                         | –0.5                                  | 4.6 | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                                                          |                         | –0.5                                  | 4.6 | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> |                         | –0.5                                  | 4.6 | V    |
|                  | Output voltage range in the high or low state <sup>(2)</sup>                                |                         | –0.5                                  | 4.6 |      |
| I <sub>IK</sub>  | Input clamp current                                                                         | V <sub>I</sub> < 0      |                                       | ±20 | mA   |
| I <sub>OK</sub>  | Output clamp current                                                                        | V <sub>O</sub> < 0      |                                       | ±20 | mA   |
| I <sub>OL</sub>  | Continuous output Low current                                                               | P port, SDA             | V <sub>O</sub> = 0 to V <sub>CC</sub> | 50  | mA   |
|                  |                                                                                             | $\overline{\text{INT}}$ |                                       | 25  |      |
| I <sub>OH</sub>  | Continuous output High current                                                              | P port                  | V <sub>O</sub> = 0 to V <sub>CC</sub> | 50  | mA   |
| T <sub>stg</sub> | Storage temperature range                                                                   |                         | –65                                   | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

**THERMAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

|               |                                          |             | UNIT |
|---------------|------------------------------------------|-------------|------|
| $\theta_{JA}$ | Package thermal impedance <sup>(1)</sup> | RTW package | 37.8 |
|               |                                          | YFP package | TBD  |

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS**

|                 |                                |                                                     | MIN                 | MAX                 | UNIT |
|-----------------|--------------------------------|-----------------------------------------------------|---------------------|---------------------|------|
| V <sub>CC</sub> | Supply voltage                 |                                                     | 1.65                | 3.6                 | V    |
| V <sub>IH</sub> | High-level input voltage       | SCL, SDA, ROW0–7, COL0–9, $\overline{\text{RESET}}$ | $0.7 \times V_{CC}$ | 3.6                 | V    |
| V <sub>IL</sub> | Low-level input voltage        | SCL, SDA, ROW0–7, COL0–9, $\overline{\text{RESET}}$ | –0.5                | $0.3 \times V_{CC}$ | V    |
| I <sub>OH</sub> | High-level output current      | ROW0–7, COL0–9                                      |                     | 10                  | mA   |
| I <sub>OL</sub> | Low-level output current       | ROW0–7, COL0–9                                      |                     | 25                  | mA   |
| T <sub>A</sub>  | Operating free-air temperature |                                                     | –40                 | 85                  | °C   |

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 1.65\text{ V}$  to  $3.6\text{ V}$  (unless otherwise noted)

| PARAMETER        |                                                                          | TEST CONDITIONS                                                                                   |                            |                                        | V <sub>CCP</sub> | MIN  | TYP | MAX  | UNIT |
|------------------|--------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|----------------------------|----------------------------------------|------------------|------|-----|------|------|
| V <sub>IK</sub>  | Input diode clamp voltage                                                | I <sub>I</sub> = −18 mA                                                                           |                            |                                        | 1.65 V to 3.6 V  | −1.2 |     |      | V    |
| V <sub>POR</sub> | Power-on reset voltage                                                   | V <sub>I</sub> = V <sub>CCP</sub> or GND, I <sub>O</sub> = 0                                      |                            |                                        | 1.65 V to 3.6 V  | 1    |     | 1.4  | V    |
| V <sub>OH</sub>  | ROW0–7, COL0–9 high-level output voltage                                 | I <sub>OH</sub> = −1 mA                                                                           |                            |                                        | 1.65 V           | 1.25 |     |      | V    |
|                  |                                                                          | I <sub>OH</sub> = −8 mA                                                                           |                            |                                        | 1.65 V           | 1.2  |     |      |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 2.3 V            | 1.8  |     |      |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 3 V              | 2.6  |     |      |      |
|                  |                                                                          | I <sub>OH</sub> = −10 mA                                                                          |                            |                                        | 1.65 V           | 1.1  |     |      |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 2.3 V            | 1.7  |     |      |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 3 V              | 2.5  |     |      |      |
| V <sub>OL</sub>  | ROW0–7, COL0–9 low-level output voltage                                  | I <sub>OL</sub> = 1 mA                                                                            |                            |                                        | 1.65 V           |      |     | 0.4  | V    |
|                  |                                                                          | I <sub>OL</sub> = 8 mA                                                                            |                            |                                        | 1.65 V           |      |     | 0.45 |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 2.3 V            |      |     | 0.25 |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 3 V              |      |     | 0.25 |      |
|                  |                                                                          | I <sub>OL</sub> = 10 mA                                                                           |                            |                                        | 1.65 V           |      |     | 0.6  |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 2.3 V            |      |     | 0.3  |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 3 V              |      |     | 0.25 |      |
| I <sub>OL</sub>  | SDA                                                                      | V <sub>OL</sub> = 0.4 V                                                                           |                            |                                        | 1.65 V to 3.6 V  | 3    |     |      | mA   |
|                  | $\overline{\text{INT}}$ and $\overline{\text{CAD\_INT}}$                 | V <sub>OL</sub> = 0.4 V                                                                           |                            |                                        | 1.65 V to 3.6 V  | 3    |     |      |      |
| I <sub>I</sub>   | $\overline{\text{SCL}}$ , SDA, ROW0–7, COL0–9, $\overline{\text{RESET}}$ | V <sub>I</sub> = V <sub>CCi</sub> or GND                                                          |                            |                                        | 1.65 V to 3.6 V  |      |     | 1    | μA   |
| r <sub>INT</sub> | ROW0–7, COL0–9                                                           |                                                                                                   |                            |                                        |                  | 105  |     |      | kΩ   |
| I <sub>CC</sub>  |                                                                          | V <sub>I</sub> on SDA, ROW0–7, COL0–9 = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, | f <sub>SCL</sub> = 0 kHz   | Oscillator OFF                         | 1.65 V to 3.6 V  |      |     | 7    | μA   |
|                  |                                                                          |                                                                                                   |                            | Oscillator ON                          |                  |      |     | 18   |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 400 kHz | 1 key press                            | 1.65 V           |      |     | 50   |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 3.6 V            |      |     | 90   |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 1 MHz   |                                        | 1.65 V           |      |     | 65   |      |
|                  |                                                                          |                                                                                                   |                            |                                        | 3.6 V            |      |     | 153  |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 400 kHz | GPI low (pullup enable) <sup>(1)</sup> | 1.65 V to 3.6 V  |      |     | 55   |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 1 MHz   |                                        |                  |      |     | 65   |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 400 kHz | GPI low (pullup disable)               |                  |      |     | 15   |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 1 MHz   |                                        |                  |      |     | 24   |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 400 kHz | 1 GPO active                           |                  |      |     | 55   |      |
|                  |                                                                          |                                                                                                   | f <sub>SCL</sub> = 1 MHz   |                                        |                  |      |     | 65   |      |
| C <sub>I</sub>   | SCL                                                                      | V <sub>I</sub> = V <sub>CCi</sub> or GND                                                          |                            |                                        | 1.65 V to 3.6 V  | 6    |     | 8    | pF   |
| C <sub>io</sub>  | SDA                                                                      | V <sub>IO</sub> = V <sub>CC</sub> or GND                                                          |                            |                                        | 1.65 V to 3.6 V  | 10   |     | 12.5 | pF   |
|                  | ROW0–7, COL0–9                                                           |                                                                                                   |                            |                                        |                  | 5    |     | 6    |      |

(1) Assumes that one GPIO is enabled.

## I<sup>2</sup>C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 13](#))

|                |                                                                            | STANDARD MODE<br>I <sup>2</sup> C BUS |      | FAST MODE<br>I <sup>2</sup> C BUS |     | FAST MODE PLUS (FM+)<br>I <sup>2</sup> C BUS |      | UNIT |
|----------------|----------------------------------------------------------------------------|---------------------------------------|------|-----------------------------------|-----|----------------------------------------------|------|------|
|                |                                                                            | MIN                                   | MAX  | MIN                               | MAX | MIN                                          | MAX  |      |
| $f_{scl}$      | I <sup>2</sup> C clock frequency                                           | 0                                     | 100  | 0                                 | 400 | 0                                            | 1000 | kHz  |
| $t_{sch}$      | I <sup>2</sup> C clock high time                                           | 4                                     |      | 0.6                               |     | 0.26                                         |      | μs   |
| $t_{scl}$      | I <sup>2</sup> C clock low time                                            | 4.7                                   |      | 1.3                               |     | 0.5                                          |      | μs   |
| $t_{sp}$       | I <sup>2</sup> C spike time                                                |                                       | 50   |                                   | 50  |                                              | 50   | ns   |
| $t_{sds}$      | I <sup>2</sup> C serial data setup time                                    | 250                                   |      | 100                               |     | 50                                           |      | ns   |
| $t_{sdh}$      | I <sup>2</sup> C serial data hold time                                     | 0                                     |      | 0                                 |     | 0                                            |      | ns   |
| $t_{icr}$      | I <sup>2</sup> C input rise time                                           |                                       | 1000 | $20 + 0.1C_b^{(1)}$               | 300 |                                              | 120  | ns   |
| $t_{icf}$      | I <sup>2</sup> C input fall time                                           |                                       | 300  | $20 + 0.1C_b^{(1)}$               | 300 |                                              | 120  | ns   |
| $t_{ocf}$      | I <sup>2</sup> C output fall time; 10 pF to 400 pF bus                     |                                       | 300  | $20 + 0.1C_b^{(1)}$               | 300 |                                              | 120  | μs   |
| $t_{buf}$      | I <sup>2</sup> C bus free time between Stop and Start                      | 4.7                                   |      | 1.3                               |     | 0.5                                          |      | μs   |
| $t_{sts}$      | I <sup>2</sup> C Start or repeater Start condition setup time              | 4.7                                   |      | 0.6                               |     | 0.26                                         |      | μs   |
| $t_{sth}$      | I <sup>2</sup> C Start or repeater Start condition hold time               | 4                                     |      | 0.6                               |     | 0.26                                         |      | μs   |
| $t_{sps}$      | I <sup>2</sup> C Stop condition setup time                                 | 4                                     |      | 0.6                               |     | 0.26                                         |      | μs   |
| $t_{vd(data)}$ | Valid data time; SCL low to SDA output valid                               |                                       | 1    |                                   | 0.9 |                                              | 0.45 | μs   |
| $t_{vd(ack)}$  | Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low |                                       | 1    |                                   | 0.9 |                                              | 0.45 | μs   |

(1)  $C_b$  = total capacitance of one bus line in pF

## RESET TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 16](#))

|             |                      | STANDARD MODE, FAST<br>MODE, FAST MODE PLUS<br>(FM+)<br>I <sup>2</sup> C BUS |     | UNIT |
|-------------|----------------------|------------------------------------------------------------------------------|-----|------|
|             |                      | MIN                                                                          | MAX |      |
| $t_W$       | Reset pulse duration | 120 <sup>(1)</sup>                                                           |     | μs   |
| $t_{REC}$   | Reset recovery time  | 120 <sup>(1)</sup>                                                           |     | μs   |
| $t_{RESET}$ | Time to reset        | 120 <sup>(1)</sup>                                                           |     | μs   |

(1) The GPIO debounce circuit uses each GPIO input which passes through a two-stage register circuit. Both registers are clocked by the same clock signal, presumably free-running, with a nominal period of 50μs. When an input changes state, the new state is clocked into the first stage on one clock transition. On the next same-direction transition, if the input state is still the same as the previously clocked state, the signal is clocked into the second stage, and then on to the remaining circuits. Since the inputs are asynchronous to the clock, it will take anywhere from zero to 50 μsec after the input transition to clock the signal into the first stage. Therefore, the total debounce time may be as long as 100 μsec. Finally, to account for a slow clock, the spec further guard-banded at 120 μsec.

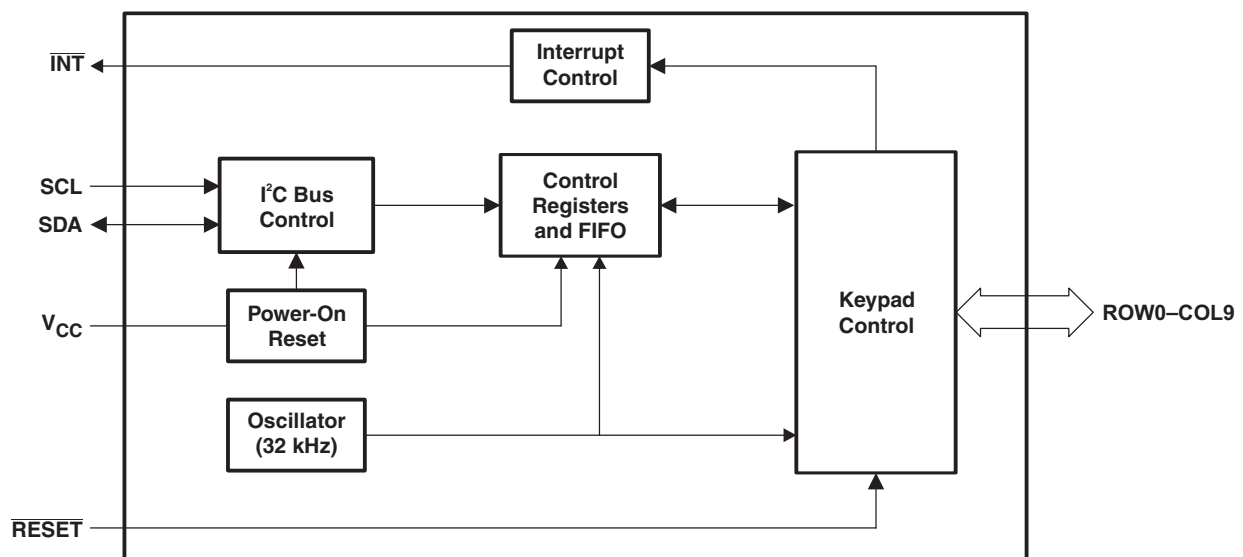
## SWITCHING CHARACTERISTICS

| PARAMETER                           |                                     | FROM           | TO                                    | STANDARD MODE, FAST MODE, FAST MODE PLUS (FM+) I <sup>2</sup> C BUS |     | UNIT    |
|-------------------------------------|-------------------------------------|----------------|---------------------------------------|---------------------------------------------------------------------|-----|---------|
|                                     |                                     |                |                                       | MIN                                                                 | MAX |         |
| $t_{IV}$ Interrupt valid time       | Key event or Key unlock or Overflow | ROW0–7, COL0–9 | $\overline{INT}$                      | 20                                                                  | 60  | $\mu s$ |
|                                     | GPI_INT with Debounce_DIS_Low       |                |                                       | 40                                                                  | 120 |         |
|                                     | GPI_INT with Debounce_DIS_High      |                |                                       | 10                                                                  | 30  |         |
|                                     | CAD_INT                             |                | $\overline{INT}, \overline{CAD\_INT}$ | 20                                                                  | 60  |         |
| $t_{IR}$ Interrupt reset delay time |                                     | SCL            | $\overline{INT}$                      | 200                                                                 |     | ns      |
|                                     |                                     | SCL            | $\overline{CAD\_INT}$                 |                                                                     |     |         |
| $t_{PV}$ Output data valid          |                                     | SCL            | ROW0–7, COL0–9                        | 400                                                                 |     | ns      |
| $t_{PS}$ Input data setup time      |                                     | P port         | SCL                                   | 0                                                                   |     | ns      |
| $t_{PH}$ Input data hold time       |                                     | P port         | SCL                                   | 300                                                                 |     | ns      |

## KEYPAD SWITCHING CHARACTERISTICS

| PARAMETER                      | STANDARD MODE, FAST MODE, FAST MODE PLUS (FM+) I <sup>2</sup> C BUS |     | UNIT    |
|--------------------------------|---------------------------------------------------------------------|-----|---------|
|                                | MIN                                                                 | MAX |         |
| Key press to detection delay   |                                                                     | 25  | $\mu s$ |
| Key release to detection delay |                                                                     | 25  | $\mu s$ |
| Keypad unlock timer            |                                                                     | 7   | s       |
| Keypad interrupt mask timer    |                                                                     | 31  | s       |
| Debounce                       |                                                                     | 60  | ms      |

## LOGIC DIAGRAM (POSITIVE LOGIC)



At power on, the GPIOs (ROW0–7 and COL0–9) are configured as inputs with internal 100-k $\Omega$  pullups enabled. However, the system master can enable the GPIOs to function as inputs, outputs or as part of the keypad matrix. GPIOs not used for keypad control can be used to support other control features in the application.

ROW7–ROW0 are configured as inputs in GPIO mode with a push-pull structure, at power-on. In keyscan mode, each has an open-drain structure with a 100-k $\Omega$  pullup resistor and is used as an input.

COL9–COL0 are configured as inputs in GPIO mode with a push-pull structure, at power on. In keyscan mode, each has an open-drain structure and is used as an output.

The system master can reset the TCA8418E in the event of a timeout or other improper operation by asserting a low in the /RESET input, while keeping the  $V_{CC}$  at its operating level.

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin low for a minimum of  $t_W$ . The TCA8418E registers and I<sup>2</sup>C/SMBus state machine are changed to their default state once RESET is low (0). When RESET is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to VCC, if no active connection is used.

The power-on reset puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine. The  $\overline{\text{RESET}}$  pin causes the same reset/initialization to occur without depowering the part. The  $\overline{\text{RESET}}$  pin can also be used as a shutdown pin, if the phone is closed.

The open-drain interrupt ( $\overline{\text{INT}}$ ) output is used to indicate to the system master that an input state (GPI or ROWs) has changed.  $\overline{\text{INT}}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote input can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the TCA8418E can remain a simple slave device.

The TCA8418E has key lock capability, which can trigger an interrupt at key presses and releases, if selected

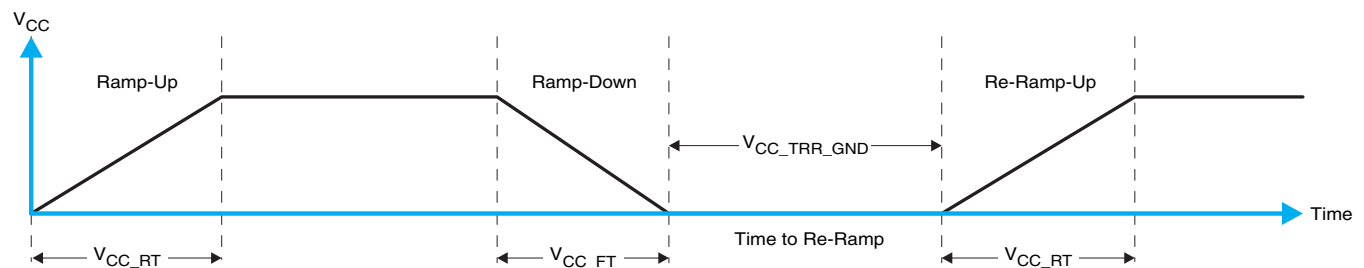
## Power-On Reset

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset holds the TCA8418E in a reset condition until  $V_{CC}$  reaches  $V_{POR}$ . At that time, the reset condition is released, and the TCA8418E registers and I<sup>2</sup>C/SMBus state machine initialize to their default states. After that,  $V_{CC}$  must be lowered below 0.2 V and back up to the operating voltage for a power-reset cycle.

## Power-On Reset Requirements

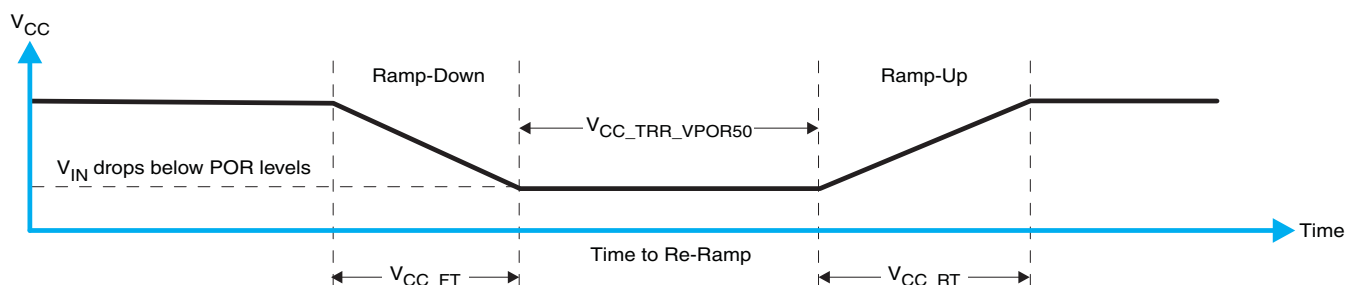
In the event of a glitch or data corruption, TCA8418E can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 1](#) and [Figure 2](#).



**Figure 1.  $V_{CC}$  is Lowered Below 0.2 V or 0 V and Then Ramped Up to  $V_{CC}$**





**Figure 2.  $V_{CC}$  is Lowered Below the POR Threshold, Then Ramped Back Up to  $V_{CC}$**

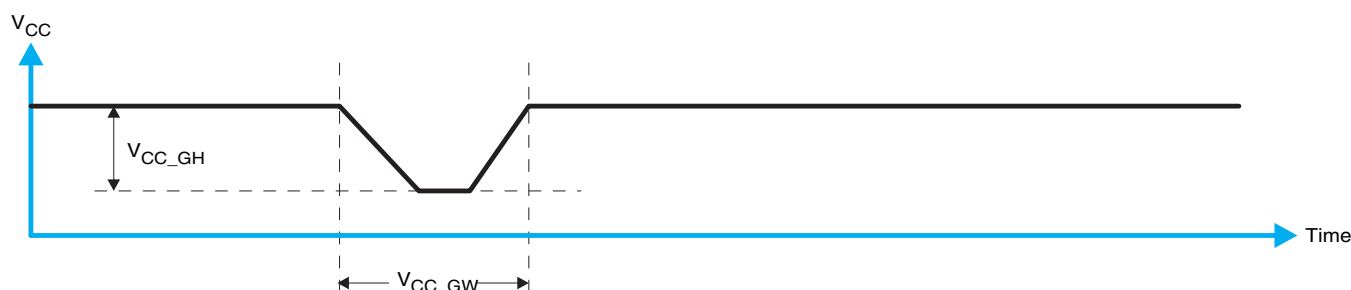
Table 1 specifies the performance of the power-on reset feature for TCA8418E for both types of power-on reset.

**Table 1. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES<sup>(1)</sup>**

| PARAMETER            |                                                                                                               |              | MIN   | TYP | MAX   | UNIT    |
|----------------------|---------------------------------------------------------------------------------------------------------------|--------------|-------|-----|-------|---------|
| $V_{CC\_FT}$         | Fall rate                                                                                                     | See Figure 1 | 1     |     | 100   | ms      |
| $V_{CC\_RT}$         | Rise rate                                                                                                     | See Figure 1 | 0.01  |     | 100   | ms      |
| $V_{CC\_TRR\_GND}$   | Time to re-ramp (when $V_{CC}$ drops to GND)                                                                  | See Figure 1 | 0.001 |     |       | ms      |
| $V_{CC\_TRR\_POR50}$ | Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV)                                               | See Figure 2 | 0.001 |     |       | ms      |
| $V_{CC\_GH}$         | Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s | See Figure 3 |       |     | 1.2   | V       |
| $V_{CC\_GW}$         | Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCX}$              | See Figure 3 |       |     |       | $\mu$ s |
| $V_{PORF}$           | Voltage trip point of POR on falling $V_{CC}$                                                                 |              | 0.767 |     | 1.144 | V       |
| $V_{PORR}$           | Voltage trip point of POR on rising $V_{CC}$                                                                  |              | 1.033 |     | 1.428 | V       |

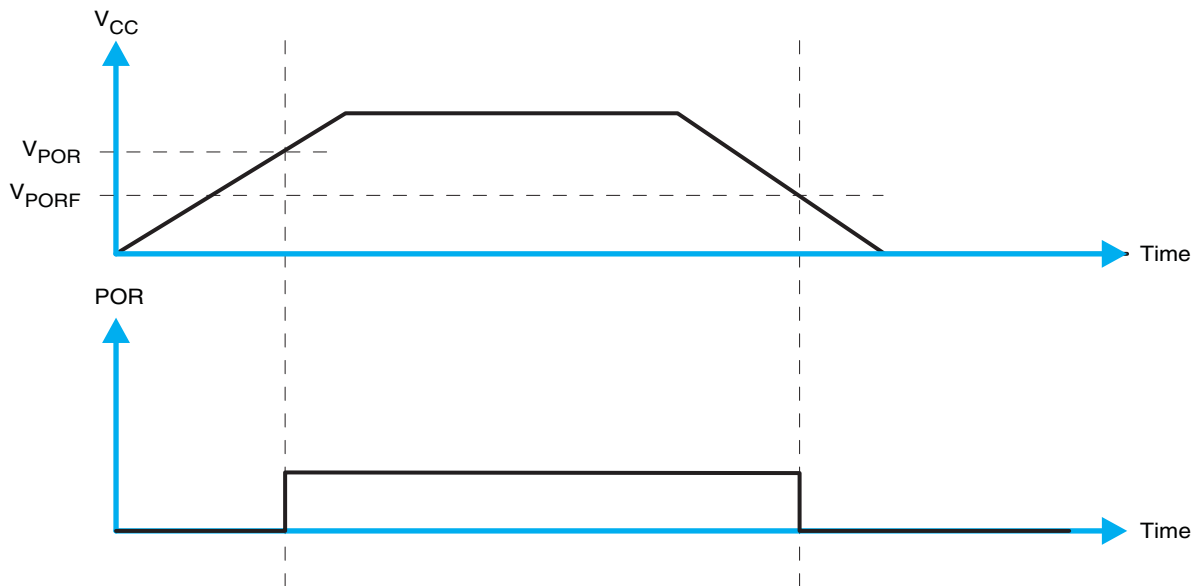
(1)  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 3 and Table 1 provide more information on how to measure these specifications.



**Figure 3. Glitch Width and Glitch Height**

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 4 and Table 1 provide more details on this specification.

Figure 4.  $V_{POR}$ 

For proper operation of the power-on reset feature, use as directed in the figures and table above.

## Interrupt Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time  $t_{iv}$ , the signal  $\overline{INT}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{INT}$ .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

The  $\overline{INT}$  output has an open-drain structure and requires a pullup resistor to  $V_{CC}$  depending on the application. If the  $\overline{INT}$  signal is connected back to the processor that provides the SCL signal to the TCA64xxA, then the  $\overline{INT}$  pin has to be connected to  $V_{CC}$ . If not, the  $\overline{INT}$  pin can be connected to  $V_{CCP}$ .

For more information on the interrupt output feature, see [Control Register and Command Byte](#) and Typical Applications.

## 50 Micro-second Interrupt Configuration

The TCA8418 provides the capability of deasserting the interrupt for 50  $\mu$ s while there is a pending event. When the  $\overline{INT\_CFG}$  bit in Register 0x01 is set, any attempt to clear the interrupt bit while the interrupt pin is already asserted results in a 50  $\mu$ s deassertion. When the  $\overline{INT\_CFG}$  bit is cleared, processor interrupt remains asserted if the host tries to clear the interrupt. This feature is particularly useful for software development and edge triggering applications.

## I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see [Figure 5](#)). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

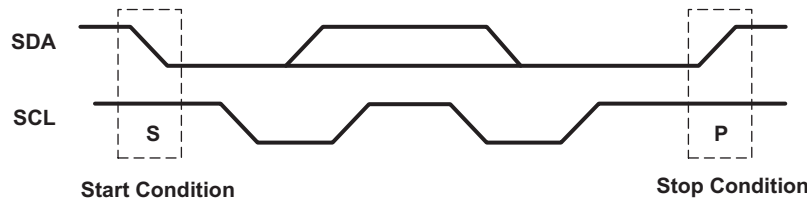
After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see [Figure 6](#)).

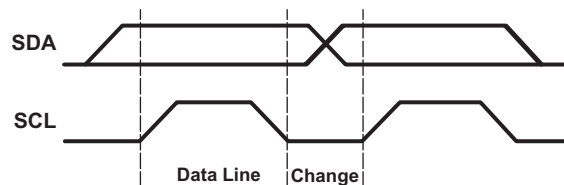
A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 5](#)).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 7](#)). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

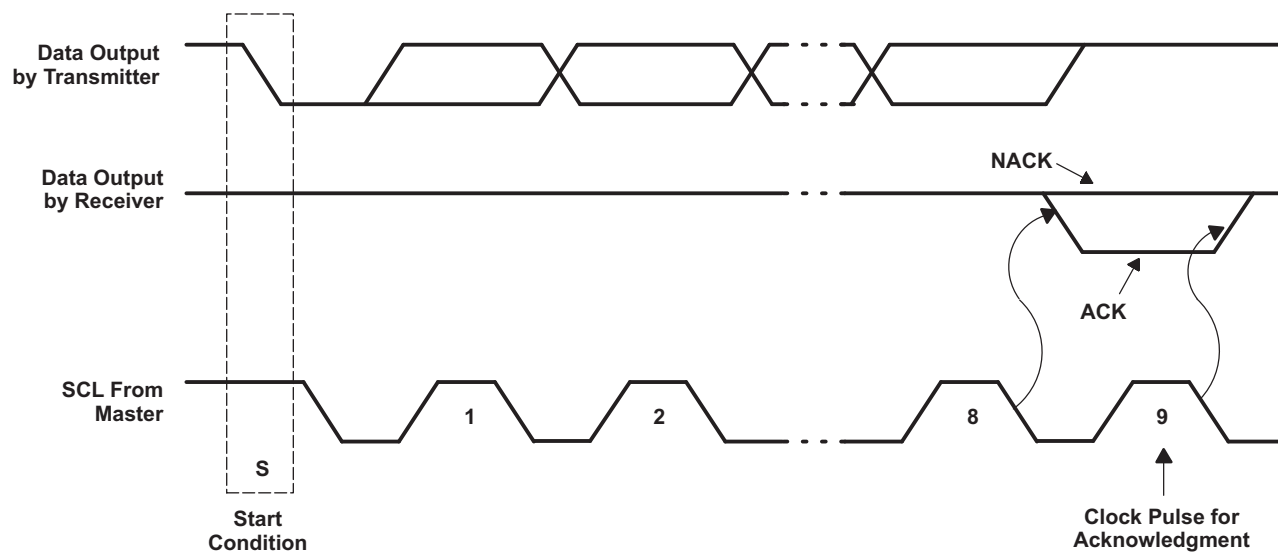
A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.



**Figure 5. Definition of Start and Stop Conditions**



**Figure 6. Bit Transfer**



**Figure 7. Acknowledgment on the I<sup>2</sup>C Bus**

## Device Address

The address of the TCA8418E is shown in [Table 2](#).

**Table 2.**

| BYTE                           | BIT     |   |   |   |   |   |   |         |
|--------------------------------|---------|---|---|---|---|---|---|---------|
|                                | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
| I <sup>2</sup> C slave address | 0       | 1 | 1 | 0 | 1 | 0 | 0 | R/W     |

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

## Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the TCA8418E. The command byte indicates the register that will be updated with information. All registers can be read and written to by the system master.

[Table 3](#) shows all the registers within this device and their descriptions. The default value in all registers is 0.

**Table 3. Register Descriptions**

| ADDRESS | REGISTER NAME  | REGISTER DESCRIPTION                                           | 7         | 6            | 5              | 4          | 3                    | 2             | 1           | 0         |
|---------|----------------|----------------------------------------------------------------|-----------|--------------|----------------|------------|----------------------|---------------|-------------|-----------|
| 0x00    | Reserved       | Reserved                                                       |           |              |                |            |                      |               |             |           |
| 0x01    | CFG            | Configuration register (interrupt processor interrupt enables) | AI        | GPI_E_CGF    | OVR_FL<br>OW_M | INT_CFG    | OVR_F<br>LOW_I<br>EN | K_LC<br>K_IEN | GPI_IE<br>N | KE_IEN    |
| 0x02    | INT_STAT       | Interrupt status register                                      | N/A<br>0  | N/A<br>0     | N/A<br>0       | N/A<br>0   | OVR_F<br>LOW_I<br>NT | K_LC<br>K_INT | GPI_<br>INT | K_<br>INT |
| 0x03    | KEY_LCK_EC     | Key lock and event counter register                            | N/A<br>0  | K_LCK<br>_EN | LCK2           | LCK1       | KLEC3                | KLEC<br>2     | KLEC1       | KLEC0     |
| 0x04    | KEY_EVENT_A    | Key event register A                                           | KEA7<br>0 | KEA6<br>0    | KEA5<br>0      | KEA4<br>0  | KEA3<br>0            | KEA2<br>0     | KEA1<br>0   | KEA0<br>0 |
| 0x05    | KEY_EVENT_B    | Key event register B                                           | KEB7<br>0 | KEB6<br>0    | KEB5<br>0      | KEB4<br>0  | KEB3<br>0            | KEB2<br>0     | KEB1<br>0   | KEB0<br>0 |
| 0x06    | KEY_EVENT_C    | Key event register C                                           | KEC7<br>0 | KEC6<br>0    | KEC5<br>0      | KEC4<br>0  | KEC3<br>0            | KEC2<br>0     | KEC1<br>0   | KEC0<br>0 |
| 0x07    | KEY_EVENT_D    | Key event register D                                           | KED7<br>0 | KED6<br>0    | KED5<br>0      | KED4<br>0  | KED3<br>0            | KED2<br>0     | KED1<br>0   | KED0<br>0 |
| 0x08    | KEY_EVENT_E    | Key event register E                                           | KEE7<br>0 | KEE6<br>0    | KEE5<br>0      | KEE4<br>0  | KEE3<br>0            | KEE2<br>0     | KEE1<br>0   | KEE0<br>0 |
| 0x09    | KEY_EVENT_F    | Key event register F                                           | KEF7<br>0 | KEF6<br>0    | KEF5<br>0      | KEF4<br>0  | KEF3<br>0            | KEF2<br>0     | KEF1<br>0   | KEF0<br>0 |
| 0x0A    | KEY_EVENT_G    | Key event register G                                           | KEG7<br>0 | KEG6<br>0    | KEG5<br>0      | KEG4<br>0  | KEG3<br>0            | KEG2<br>0     | KEG1<br>0   | KEG0<br>0 |
| 0x0B    | KEY_EVENT_H    | Key event register H                                           | KEH7<br>0 | KEH6<br>0    | KEH5<br>0      | KEH4<br>0  | KEH3<br>0            | KEH2<br>0     | KEH1<br>0   | KEH0<br>0 |
| 0x0C    | KEY_EVENT_I    | Key event register I                                           | KEI7<br>0 | KEI6<br>0    | KEI5<br>0      | KEI4<br>0  | KEI3<br>0            | KEI2<br>0     | KEI1<br>0   | KEI0<br>0 |
| 0x0D    | KEY_EVENT_J    | Key event register J                                           | KEJ7<br>0 | KEJ6<br>0    | KEJ5<br>0      | KEJ64<br>0 | KEJ3<br>0            | KEJ2<br>0     | KEJ1<br>0   | KEJ0<br>0 |
| 0x0E    | KP_LCK_TIMER   | Keypad lock 1 to lock 2 timer                                  | KL7       | KL6          | KL5            | KL4        | KL3                  | KL2           | KL1         | KL0       |
| 0x0F    | Unlock1        | Unlock key 1                                                   | UK1_7     | UK1_6        | UK1_5          | UK1_4      | UK1_3                | UK1_<br>2     | UK1_1       | UK1_0     |
| 0x10    | Unlock2        | Unlock key2                                                    | UK2_7     | UK2_6        | UK2_5          | UK2_4      | UK2_3                | UK2_<br>2     | UK2_1       | UK2_0     |
| 0x11    | GPIO_INT_STAT1 | GPIO interrupt status                                          | R7IS<br>0 | R6IS<br>0    | R5IS<br>0      | R4IS<br>0  | R3IS<br>0            | R2IS<br>0     | R1IS<br>0   | R0IS<br>0 |
| 0x12    | GPIO_INT_STAT2 | GPIO interrupt status                                          | C7IS<br>0 | C6IS<br>0    | C5IS<br>0      | C4IS<br>0  | C3IS<br>0            | C2IS<br>0     | C1IS<br>0   | C0IS<br>0 |

**Table 3. Register Descriptions (continued)**

| ADDRESS | REGISTER NAME                           | REGISTER DESCRIPTION                                | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|---------|-----------------------------------------|-----------------------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0×13    | GPIO_INT_STAT3                          | GPIO interrupt status                               | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9IS<br>0 | C8IS<br>0 |
| 0×14    | GPIO_DAT_STAT1<br>(read twice to clear) | GPIO data status                                    | R7DS      | R6DS      | R5DS      | R4DS      | R3DS      | R2DS      | R1DS      | R0DS      |
| 0×15    | GPIO_DAT_STAT2<br>(read twice to clear) | GPIO data status                                    | C7DS      | C6DS      | C5DS      | C4DS      | C3DS      | C2DS      | C1DS      | C0DS      |
| 0×16    | GPIO_DAT_STAT3<br>(read twice to clear) | GPIO data status                                    | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9DS      | C8DS      |
| 0×17    | GPIO_DAT_OUT1                           | GPIO data out                                       | R7DO<br>0 | R6DO<br>0 | R5DO<br>0 | R4DO<br>0 | R3DO<br>0 | R2DO<br>0 | R1DO<br>0 | R0DO<br>0 |
| 0×18    | GPIO_DAT_OUT2                           | GPIO data out                                       | C7DO<br>0 | C6DO<br>0 | C5DO<br>0 | C4DO<br>0 | C3DO<br>0 | C2DO<br>0 | C1DO<br>0 | C0DO<br>0 |
| 0×19    | GPIO_DAT_OUT3                           | GPIO data out                                       | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9DO<br>0 | C8DO<br>0 |
| 0×1A    | GPIO_INT_EN1                            | GPIO interrupt enable                               | R7IE<br>0 | R6IE<br>0 | R5IE<br>0 | R4IE<br>0 | R3IE<br>0 | R2IE<br>0 | R1IE<br>0 | R0IE<br>0 |
| 0×1B    | GPIO_INT_EN2                            | GPIO interrupt enable                               | C7IE<br>0 | C6IE<br>0 | C5IE<br>0 | C4IE<br>0 | C3IE<br>0 | C2IE<br>0 | C1IE<br>0 | C0IE<br>0 |
| 0×1C    | GPIO_INT_EN3                            | GPIO interrupt enable                               | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9IE<br>0 | C8IE<br>0 |
| 0×1D    | KP_GPIO1                                | Keypad or GPIO selection<br>0: GPIO<br>1: KP matrix | ROW7<br>0 | ROW6<br>0 | ROW5<br>0 | ROW4<br>0 | ROW3<br>0 | ROW2<br>0 | ROW1<br>0 | ROW0<br>0 |
| 0×1E    | KP_GPIO2                                | Keypad or GPIO selection<br>0: GPIO<br>1: KP matrix | COL7<br>0 | COL6<br>0 | COL5<br>0 | COL4<br>0 | COL3<br>0 | COL2<br>0 | COL1<br>0 | COL0<br>0 |
| 0×1F    | KP_GPIO3                                | Keypad or GPIO selection<br>0: GPIO<br>1: KP matrix | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | COL9<br>0 | COL8<br>0 |
| 0×20    | GPI_EM1                                 | GPI event mode 1                                    | ROW7<br>0 | ROW6<br>0 | ROW5<br>0 | ROW4<br>0 | ROW3<br>0 | ROW2<br>0 | ROW1<br>0 | ROW0<br>0 |
| 0×21    | GPI_EM2                                 | GPI event mode 2                                    | COL7<br>0 | COL6<br>0 | COL5<br>0 | COL4<br>0 | COL3<br>0 | COL2<br>0 | COL1<br>0 | COL0<br>0 |
| 0×22    | GPI_EM3                                 | GPI event mode 3                                    | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | COL9<br>0 | COL8<br>0 |
| 0×23    | GPIO_DIR1                               | GPIO data direction<br>0: input<br>1: output        | R7DD<br>0 | R6DD<br>0 | R5DD<br>0 | R4DD<br>0 | R3DD<br>0 | R2DD<br>0 | R1DD<br>0 | R0DD<br>0 |
| 0×24    | GPIO_DIR2                               | GPIO data direction<br>0: input<br>1: output        | C7DD<br>0 | C6DD<br>0 | C5DD<br>0 | C4DD<br>0 | C3DD<br>0 | C2DD<br>0 | C1DD<br>0 | C0DD<br>0 |
| 0×25    | GPIO_DIR3                               | GPIO data direction<br>0: input<br>1: output        | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9DD<br>0 | C8DD<br>0 |
| 0×26    | GPIO_INT_LVL 1                          | GPIO edge/level detect<br>0: low<br>1: high         | R7IL<br>0 | R6IL<br>0 | R5IL<br>0 | R4IL<br>0 | R3IL<br>0 | R2IL<br>0 | R1IL<br>0 | R0IL<br>0 |
| 0×27    | GPIO_INT_LVL 2                          | GPIO edge/level detect<br>0: low<br>1: high         | C7IL<br>0 | C6IL<br>0 | C5IL<br>0 | C4IL<br>0 | C3IL<br>0 | C2IL<br>0 | C1IL<br>0 | C0IL<br>0 |

**Table 3. Register Descriptions (continued)**

| ADDRESS | REGISTER NAME  | REGISTER DESCRIPTION                                   | 7                  | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|---------|----------------|--------------------------------------------------------|--------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0x28    | GPIO_INT_LVL 3 | GPIO edge/level detect<br>0: low<br>1: high            | N/A<br>0           | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9IL<br>0 | C8IL<br>0 |
| 0x29    | DEBOUNCE_DIS 1 | Debounce disable<br>0: enabled<br>1: disabled          | R7DD<br>0          | R6DD<br>0 | R5DD<br>0 | R4DD<br>0 | R3DD<br>0 | R2DD<br>0 | R1DD<br>0 | R0DD<br>0 |
| 0x2A    | DEBOUNCE_DIS 2 | Debounce disable<br>0: enabled<br>1: disabled          | C7DD<br>0          | C6DD<br>0 | C5DD<br>0 | C4DD<br>0 | C3DD<br>0 | C2DD<br>0 | C1DD<br>0 | C0DD<br>0 |
| 0x2B    | DEBOUNCE_DIS 3 | Debounce disable<br>0: enabled<br>1: disabled          | Debounce time bits |           |           | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9DD<br>0 | C8DD<br>0 |
| 0x2C    | GPIO_PULL1     | GPIO pullup<br>0: pullup enabled<br>1: pullup disabled | R7PD<br>0          | R6PD<br>0 | R5PD<br>0 | R4PD<br>0 | R3PD<br>0 | R2PD<br>0 | R1PD<br>0 | R0PD<br>0 |
| 0x2D    | GPIO_PULL2     | GPIO pullup<br>0: pullup enabled<br>1: pullup disabled | C7PD<br>0          | C6PD<br>0 | C5PD<br>0 | C4PD<br>0 | C3PD<br>0 | C2PD<br>0 | C1PD<br>0 | C0PD<br>0 |
| 0x2E    | GPIO_PULL3     | GPIO pullup<br>0: pullup enabled<br>1: pullup disabled | N/A<br>0           | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | N/A<br>0  | C9PD<br>0 | C8PD<br>0 |
| 0x2F    | Reserved       |                                                        |                    |           |           |           |           |           |           |           |

**Configuration Register (Address 0x01)**

| BITS | NAME         | DESCRIPTION                                                                                                                                                                                                                                                                                                                                     |
|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | AI           | Auto-increment for read and write operations<br>0 = disabled<br>1 = enabled                                                                                                                                                                                                                                                                     |
| 6    | GPI_E_CFG    | GPI event mode configuration<br>0 = GPI events are tracked when keypad is locked<br>1 = GPI events are not tracked when keypad is locked                                                                                                                                                                                                        |
| 5    | OVR_FLOW_M   | Overflow mode<br>0 = disabled; overflow data is lost<br>1 = enabled.                                                                                                                                                                                                                                                                            |
| 4    | INT_CFG      | Overflow data shifts with last event pushing first event out interrupt configuration.<br>0 = processor interrupt remains asserted (or low) if host tries to clear interrupt while there is still a pending key press, key release or GPI interrupt<br>1 = processor interrupt is deasserted for 50 $\mu$ s and reassert with pending interrupts |
| 3    | OVR_FLOW_IEN | Overflow interrupt enable<br>0 = disabled<br>1 = enabled                                                                                                                                                                                                                                                                                        |
| 2    | K_LCK_IEN    | Keypad lock interrupt enable<br>0 = disabled<br>1 = enabled                                                                                                                                                                                                                                                                                     |
| 1    | GPI_IEN      | GPI interrupt enable to host processor<br>0 = disabled<br>1 = enabled<br>Can be used to mask interrupts                                                                                                                                                                                                                                         |

| BIT | NAME   | DESCRIPTION                                                                                                 |
|-----|--------|-------------------------------------------------------------------------------------------------------------|
| 0   | KE_IEN | Key events interrupt enable to host processor<br>0 = disabled<br>1 = enabled Can be used to mask interrupts |

Bit 7 in this register is used to determine the programming mode. If it is low, all data bytes are written to the registers defined command byte. If bit 7 is high, the value of the command byte is automatically incremented after the byte is written, and the next data byte is stored in the corresponding register. Registers are written in the sequence shown in [Table 3](#). Once the GPIO\_PULL3 register (0x2E) is written to, the command byte returns to 0 (Configuration register). Registers 0 and 2F are reserved and a command byte that references these registers is not acknowledged by the TCA8418E.

The keypad lock interrupt enable determines if the interrupt pin is asserted when the key lock interrupt (see [Interrupt Status Register](#)) bit is set.

#### Interrupt Status Register, INT\_STAT (Address 0x02)

| BIT | NAME         | DESCRIPTION                                                                                                                                                                                                      |
|-----|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | N/A          | Always 0                                                                                                                                                                                                         |
| 6   | N/A          | Always 0                                                                                                                                                                                                         |
| 5   | N/A          | Always 0                                                                                                                                                                                                         |
| 4   | CAD_INT      | CTRL-ALT-DEL key sequence status. Requires writing a 1 to clear interrupts.<br>0 = interrupt not detected<br>1 = interrupt detected                                                                              |
| 3   | OVR_FLOW_INT | Overflow interrupt status. Requires writing a 1 to clear interrupts.<br>0 = interrupt not detected<br>1 = interrupt detected                                                                                     |
| 2   | K_LCK_INT    | Keypad lock interrupt status. This is the interrupt to the processor when the keypad lock sequence is started. Requires writing a 1 to clear interrupts.<br>0 = interrupt not detected<br>1 = interrupt detected |
| 1   | GPI_INT      | GPI interrupt status. Requires writing a 1 to clear interrupts.<br>0 = interrupt not detected<br>1 = interrupt detected<br>Can be used to mask interrupts                                                        |
| 0   | K_INT        | Key events interrupt status. Requires writing a 1 to clear interrupts.<br>0 = interrupt not detected<br>1 = interrupt detected                                                                                   |

#### Key Lock and Event Counter Register, KEY\_LCK\_EC (Address 0x03)

| BIT | NAME     | DESCRIPTION                                                                          |
|-----|----------|--------------------------------------------------------------------------------------|
| 7   | N/A      | Always 0                                                                             |
| 6   | K_LCK_EN | Key lock enable<br>0 = disabled<br>1 = enabled                                       |
| 5   | LCK2     | Keypad lock status<br>0 = unlock (if LCK1 is 0 too)<br>1 = locked (if LCK1 is 1 too) |
| 4   | LCK1     | Keypad lock status<br>0 = unlock (if LCK2 is 0 too)<br>1 = locked (if LCK2 is 1 too) |
| 3   | KEC3     | Key event count, Bit 3                                                               |
| 2   | KEC2     | Key event count, Bit 2                                                               |



| BIT | NAME | DESCRIPTION            |
|-----|------|------------------------|
| 1   | KEC1 | Key event count, Bit 1 |
| 0   | KEC0 | Key event count, Bit 0 |

KEC[3:0]: indicates how many registers have values in it. For example, KS(0000) = 0 events, KS(0001) = 1 event and KS(1010) = 10 events. As interrupts happen (press or release), the count increases accordingly.

### Key Event Registers (FIFO), KEY\_EVENT\_A–J (Address 0x04–0x0D)

| ADDRESS | REGISTER NAME <sup>(1)</sup> | REGISTER DESCRIPTION | BIT           |           |               |           |           |               |           |               |
|---------|------------------------------|----------------------|---------------|-----------|---------------|-----------|-----------|---------------|-----------|---------------|
|         |                              |                      | 7             | 6         | 5             | 4         | 3         | 2             | 1         | 0             |
| 0x04    | KEY_EVENT_A                  | Key event register A | KEA<br>7<br>0 | KEA6<br>0 | KEA<br>5<br>0 | KEA4<br>0 | KEA3<br>0 | KEA<br>2<br>0 | KEA1<br>0 | KEA<br>0<br>0 |

(1) Only KEY\_EVENT\_A register is shown

These registers – KEY\_EVENT\_A–J – function as a FIFO stack which can store up to 10 key presses and releases. The user first checks the INT\_STAT register to see if there are any interrupts. If so, then the Key Lock and Event Counter Register (KEY\_LCK\_EC, register 0x03) is read to see how many interrupts are stored. The INT\_STAT register is then read again to ensure no new events have come in. The KEY\_EVENT\_A register is then read as many times as there are interrupts. Each time a read happens, the count in the KEY\_LCK\_EC register reduces by 1. The data in the FIFO also moves down the stack by 1 too (from KEY\_EVENT\_J to KEY\_EVENT\_A). Once all events have been read, the key event count is at 0 and then KE\_INT bit can be cleared by writing a '1' to it.

In the KEY\_EVENT\_A register, KEA[6:0] indicates the key # pressed or released. A value of 0 to 80 indicate which key has been pressed or released in a keypad matrix. Values of 97 to 114 are for GPI events.

Bit 7 or KEA[7] indicate if a key press or key release has happened. A '0' means a key release happened. A '1' means a key has been pressed (which can be cleared on a read).

For example, 3 key presses and 3 key releases are stored as 6 words in the FIFO. As each word is read, the user knows if it is a key press or key release that occurred. Key presses such as CTRL+ALT+DEL are stored as 3 simultaneous key presses. Key presses and releases generate key event interrupts. The KE\_INT bit and /INT pin will not cleared until the FIFO is cleared of all events.

All registers can be read but for the purpose of the FIFO, the user should only read KEY\_EVENT\_A register. Once all the events in the FIFO have been read, reading of KEY\_EVENT\_A register will yield a zero value.

### Keypad Lock1 to Lock2 Timer Register, KP\_LCK\_TIMER (Address 0x0E)

| ADDRESS | REGISTER NAME <sup>(1)</sup> | REGISTER DESCRIPTION          | BIT |     |     |     |     |     |     |     |
|---------|------------------------------|-------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |                              |                               | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| 0x0E    | KP_LCK_TIMER                 | Keypad lock 1 to lock 2 timer | KL7 | KL6 | KL5 | KL4 | KL3 | KL2 | KL1 | KL0 |

(1) Only KEY\_EVENT\_A register is shown

KL[2:0] are for the Lock1 to Lock2 timer

KL[7:3] are for the interrupt mask timer

The interrupt mask timer should be set for the time it takes for the LCD to dim or turn off.

### Unlock1 and Unlock2 Registers, UNLOCK1/2 (Address 0x0F)

| ADDRESS | REGISTER NAME <sup>(1)</sup> | REGISTER DESCRIPTION | BIT      |          |          |          |          |          |          |          |
|---------|------------------------------|----------------------|----------|----------|----------|----------|----------|----------|----------|----------|
|         |                              |                      | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| 0x0F    | Unlock1                      | Unlock key 1         | UK1<br>7 | UK1<br>6 | UK1<br>5 | UK1<br>4 | UK1<br>3 | UK1<br>2 | UK1<br>1 | UK1<br>0 |
| 0x10    | Unlock2                      | Unlock key 2         | UK2<br>7 | UK2<br>6 | UK2<br>5 | UK2<br>4 | UK2<br>3 | UK2<br>2 | UK2<br>1 | UK2<br>0 |

(1) Only KEY\_EVENT\_A register is shown

UK1[6:0] contains the key number used to unlock key 1

UK2[6:0] contains the key number used to unlock key 2

A '0' in either register means it is disabled. It lasts up to 7 seconds. Needs a second timer up to 31 seconds? The keypad lock interrupt mask timer generates a first interrupt (K\_INT) and then waits for a programmed time before generating a second interrupt. A second interrupt can only be generated when a timer is enabled due to an unlock sequence being pressed. The second interrupt is a key lock interrupt. When the interrupt mask timer is disabled ('0'), a key lock interrupt will trigger only when the correct and complete unlock sequence is completed.

#### **GPIO Interrupt Status Registers, GPIO\_INT\_STAT1–3 (Address 0x11–0x13)**

These registers are used to check GPIO interrupt status and are cleared on read.

#### **GPIO Data Status Registers, GPIO\_DAT\_STAT1–3 (Address 0x14–0x16)**

These registers show GPIO state when read for inputs and outputs.

#### **GPIO Data Out Registers, GPIO\_DAT\_OUT1–3 (Address 0x17–0x19)**

These registers contain GPIO data to be written to GPIO out driver; inputs are not affected. This is needed so that the value can be written prior to being set as an output.

#### **GPIO Interrupt Enable Registers, GPIO\_INT\_EN1–3 (Address 0x1A–0x1C)**

These registers enable interrupts for GP inputs only.

#### **Keypad or GPIO Selection Registers, KP\_GPIO1–3 (Address 0x1D–0x1F)**

A bit value of '0' in any of the unreserved bits puts the corresponding pin in GPIO mode. A '1' in any of these bits puts the pin in keyscan mode and configured as a row or column accordingly.

#### **GPI Event Mode Registers, GPI\_EM1–3 (Address 0x20–0x22)**

A bit value of '0' in any of the unreserved bits indicates that it is not part of the event FIFO. A '1' in any of these bits means it is part of the event FIFO. GPIO Data Direction Registers (GPIO\_DIR1-3, Register address of 0x23-0x25) A bit value of '0' in any of the unreserved bits sets the corresponding pin as an input. A '1' in any of these bits sets the pin as an output. GPIO Edge/Level Detect Registers (GPIO\_INT\_LVL1-3, Register address of 0x26-0x28) A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

#### **GPIO Data Direction Registers, GPIO\_DIR1–3 (Address 0x23–0x25)**

A bit value of '0' in any of the unreserved bits sets the corresponding pin as an input. A '1' in any of these bits sets the pin as an output. GPIO Edge/Level Detect Registers (GPIO\_INT\_LVL1-3, Register address of 0x26-0x28) A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

#### **GPIO Edge/Level Detect Registers, GPIO\_INT\_LVL1–3 (Address 0x26–0x28)**

A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

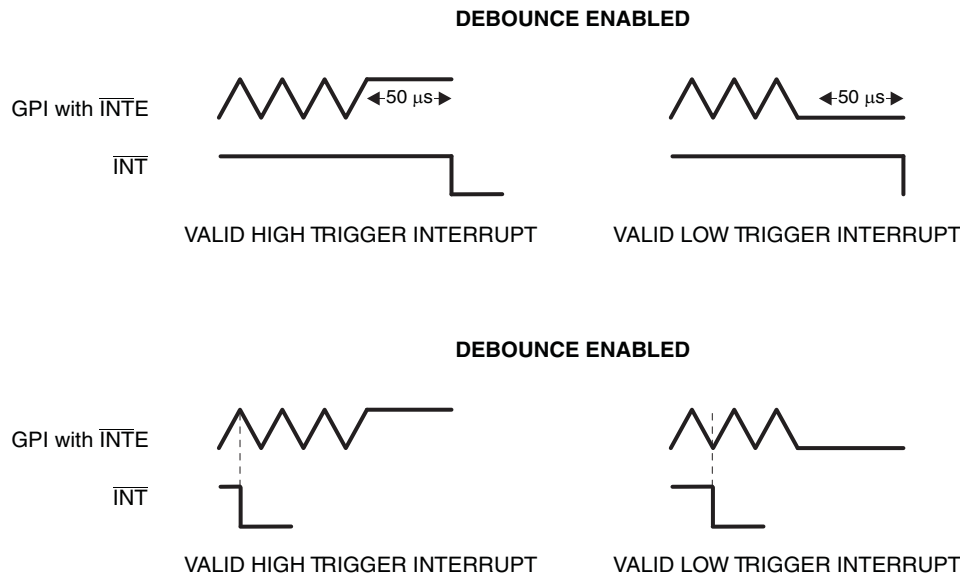
#### **Debounce Disable Registers, DEBOUNCE\_DIS1–3 (Address 0x29–0x2B)**

This is for pins configured as inputs. A bit value of '0' in any of the unreserved bits disables the debounce while a bit value of '1' enables the debounce.

In register DEBOUNCE\_DIS3 [7:5] can be used to program the value of the debounce time.

| ADDRESS | REGISTER NAME <sup>(1)</sup> | REGISTER DESCRIPTION                          | BIT                |   |   |          |          |          |           |               |
|---------|------------------------------|-----------------------------------------------|--------------------|---|---|----------|----------|----------|-----------|---------------|
|         |                              |                                               | 7                  | 6 | 5 | 4        | 3        | 2        | 1         | 0             |
| 0×2B    | DEBOUNCE_DIS 3               | Debounce disable<br>0: enabled<br>1: disabled | debounce time bits |   |   | N/A<br>0 | N/A<br>0 | N/A<br>0 | C9DD<br>0 | C8D<br>D<br>0 |

(1) Only KEY\_EVENT\_A register is shown



Debounce disable will have the same effect for GPI mode or for rows in keypad scanning mode. The reset line always has a 50-μs debounce time.

The debounce time for inputs is the time required for the input to be stable to be noticed. This time is 50 μs.

The debounce time for the keypad is for the columns only. The minimum time is 20 ms. All columns are scanned once every 20 ms to detect any key presses. Two full scans are required to see if any keys were pressed. If the first scan is done just after a key press, it will take 20 ms to detect the key press. If the first scan is done much later than the key press, it will take 40 ms to detect a key press.

### GPIO Pull Disable Register, GPIO\_PULL1–3 (Address 0×2C–0×2E)

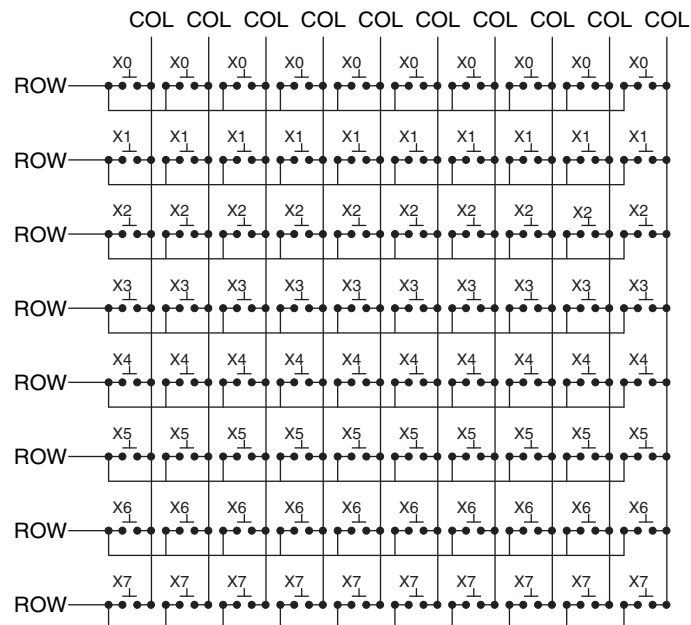
This register enables or disables pullup registers from inputs.

## Typical Application

Figure 8 shows an application in which the TCA8418E can be used.

placeholder

**Figure 8. Typical Application**



The 18 GPIOs can be configured to support up to 80 keys. The GPIOs are programmed into rows (maximum of 8) and columns (maximum of 10) to support a keypad. This is done through writing to “Keypad or GPIO Selection” registers (0x1D – 0x1F). The keypad in idle mode will be configured as Columns being driven low and Rows as inputs with pull-ups.

When there is a key press or multiple key presses (Short between Column and Row), it will trigger an internal state machine interrupt. The row that has a pressed key can be determined through reading the “GPIO Data Status” registers (0x14-0x16). After that, the state machine starts a keyscan cycle to determine the column of the key that was pressed. The state machine sets one column as an output low and all other columns as high. The state machine will then walk a zero across the applicable row to determine what keys are being pressed.

Once a key has been pressed for 10ms, the state machine will set the appropriate key/s in the Key Event Status register with the key-pressed bit set (bit 7). If the K\_IEN is set it will then set KE\_INT and generate an interrupt to the host processor. The state machine will continue to poll while there are keys pressed. If a key/s that was in the key pressed register is released for 10ms or greater, the state machine will set the appropriate keys in the Key Event Status register with the key pressed bit cleared. If K\_IEN is set it will set the K\_INT and generate an interrupt to the host processor.

After receiving an interrupt, the host processor will first read the Interrupt Status register to determine what interrupt caused the processor interrupt. It will then read the Key Event Register to see what keys were pressed/released (Bits will then automatically clear on read in those registers). The processor will then write a 1 to the interrupt bit in the interrupt register to clear it and release the interrupt to the processor. The processor can see the status of what keys are pressed at any point by reading the KEY\_EVENT\_A register (FIFO).

See [Key Event Registers \(FIFO\)](#) for more information.

When all Key\_Event Registers are full, any additional events will set the OVR\_FLOW\_INT bit to 1. This will also trigger an interrupt to the processor. When the FIFO is not full, new events are added to the next empty Key\_Event register in line. The OVR\_FLOW\_M bit sets the mode of operation during overflows. Clearing this bit will cause new incoming events to be ignored and discarded. Setting this bit will overwrite old data with new data starting with the first event.

## Keypad Lock/Unlock

This user can lock the keypad through the lock/unlock feature in this device. Once the keypad is locked, it can prevent the generation of key event interrupts and recorded key events. The unlock keys can be programmed with any value of the keys in the keypad matrix or any GPI values that are part of the key event table. When the keypad lock interrupt mask timer is enabled, the user will need to press two specific keys before an keylock interrupt is generated or keypad events are recorded. After the keypad is locked, a key event interrupt is generated any time a user presses a key. This first interrupt also triggers the processor to turn on the LCD and display the unlock message. The processor will then read the lock status register to see if the keypad is unlocked. The next interrupt (keylock interrupt) will not be generated unless both unlock keys sequences are correct. If correct Unlock keys are not pressed before the mask timer expires, the state machine will start over again.

## Ghosting

Supports multiple key presses accurately. Applications requiring three-key combinations (such as <Ctrl><Alt><Del>) must ensure that the three keys are wired in appropriate key positions to avoid ghosting (or appearing like a 4th key has been pressed)

## GPI Events

A column or row configured as GPI can be programmed to be part of the Key Event Table, hence becomes also capable of generating Key Event Interrupt. A key Event Interrupt caused by a GPI follow the same process flow as a Key Event Interrupt caused by a Key press.

GPIs configured as part of the Key Event Table allows for single key switches to be monitored as well as other GPI interrupts. As part of the Event Table, GPIs are represented with decimal value of 97 (0x61 or 1100001) and run through decimal value of 114 (0x72 or 1110010).

For a GPI that is set as active high, and is enabled in the Key Event Table, the state-machine will add an event to the event count and event table whenever that GPI goes high. If the GPI is set to active low, a transition from high to low will be considered a press and will also be added to the event count and event table. Once the interrupt state has been met, the state machine will internally set an interrupt for the opposite state programmed in the register to avoid polling for the released state, hence saving current. Once the released state is achieved, it will add it to the event table. The press and release will still be indicated by bit 7 in the event register.

The GPI Events can also be used as unlocked sequences. When the GPI\_EM bit is set, GPI events will not be tracked when the keypad is locked. GPI\_EM bit must be cleared for the GPI events to be tracked in the event counter and table when the keypad is locked.

## Bus Transactions

Data is exchanged between the master and TCA8418E through write and read commands.

## Writes

Data is transmitted to the TCA8418E by sending the device address and setting the least significant bit (LSB) to a logic 0. The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

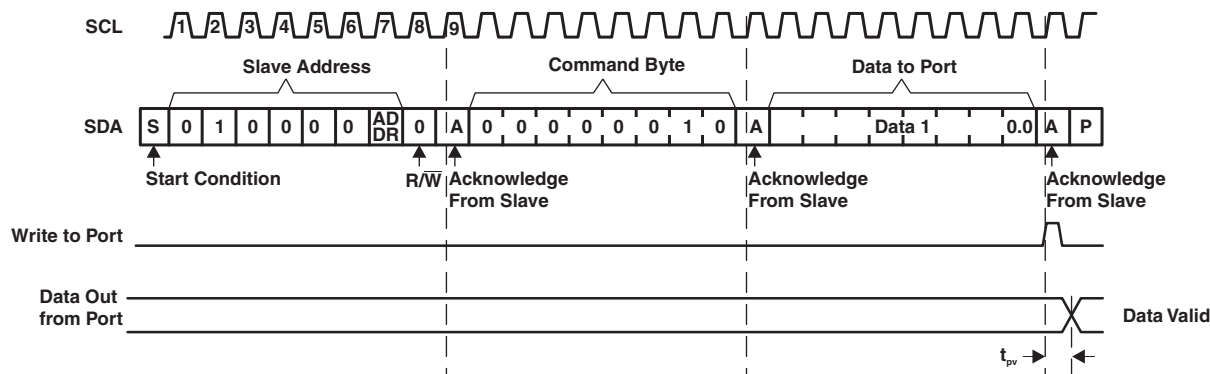


Figure 9. Write to Output Port Register

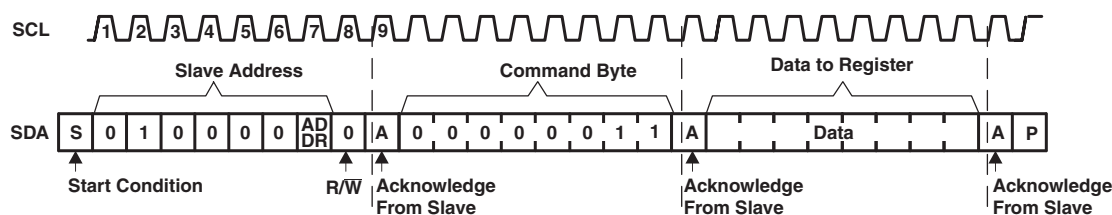


Figure 10. Write to Configuration or Polarity Inversion Register

## Reads

The bus master first must send the TCA8418E address with the LSB set to a logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA8418E (see Figure 11 and Figure 12). Data is clocked into the register on the rising edge of the ACK clock pulse.

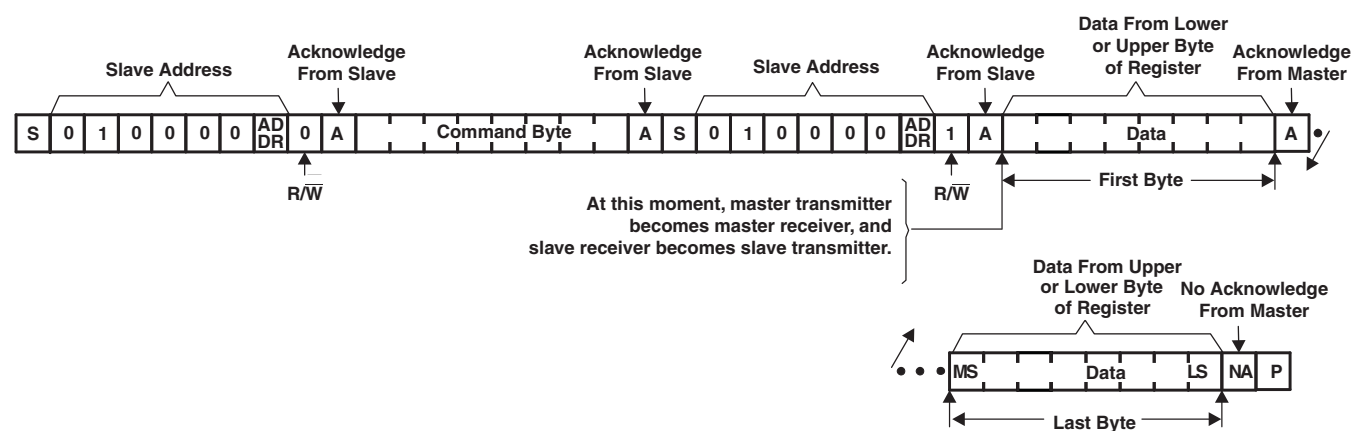


Figure 11. Read From Register

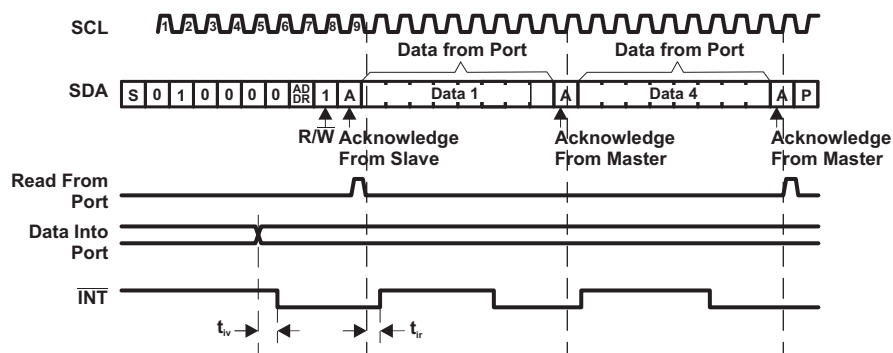
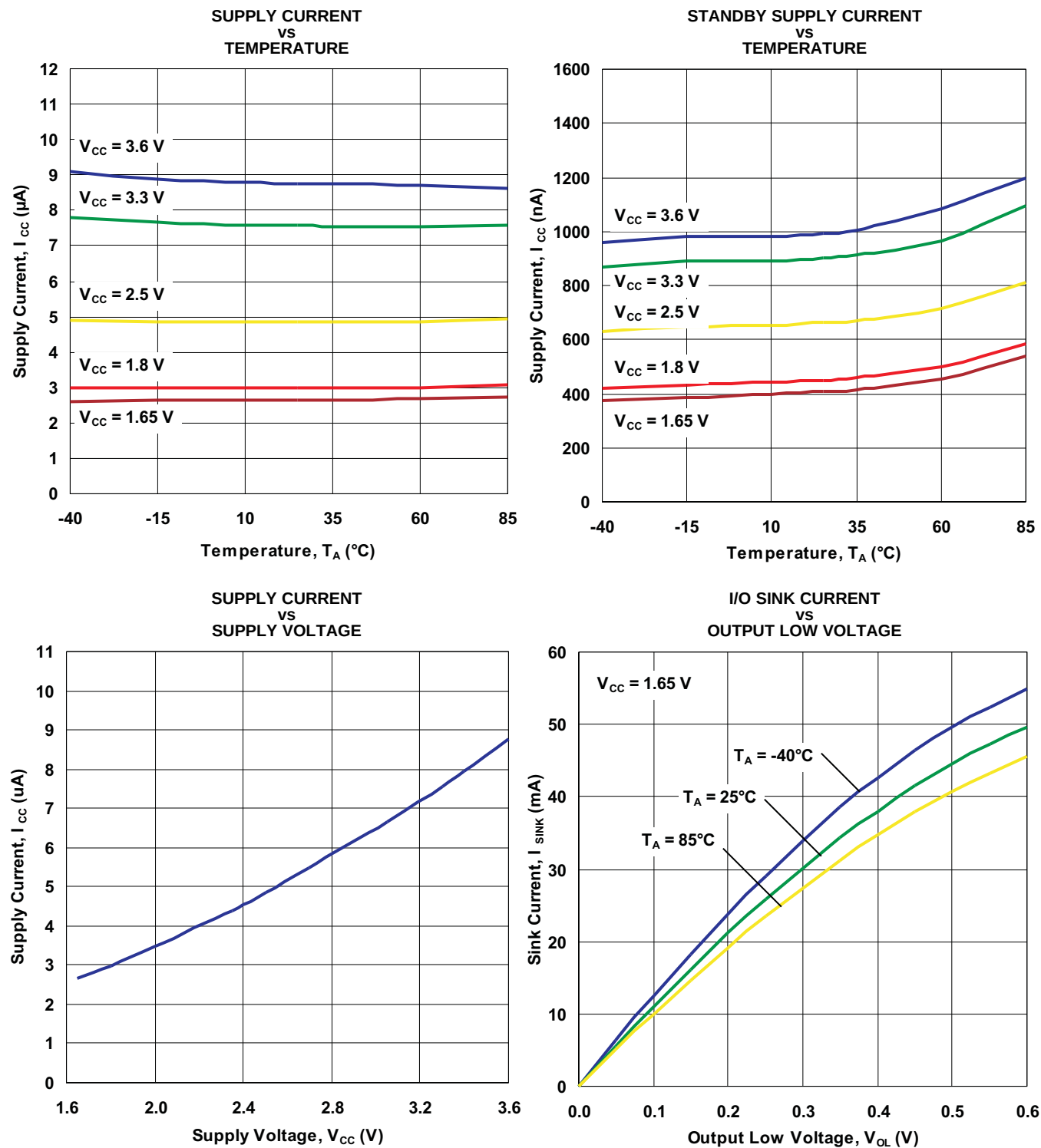


Figure 12. Read From Input Port Register

## TYPICAL CHARACTERISTICS

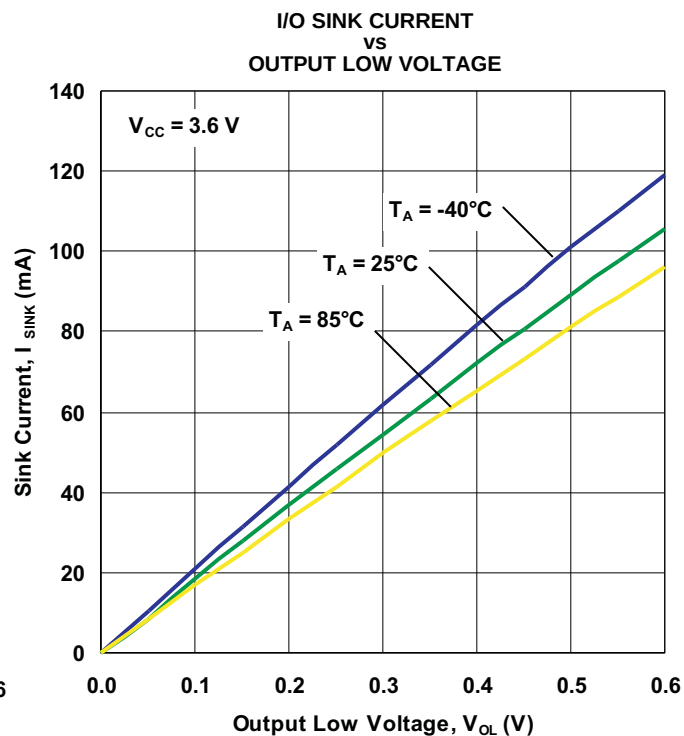
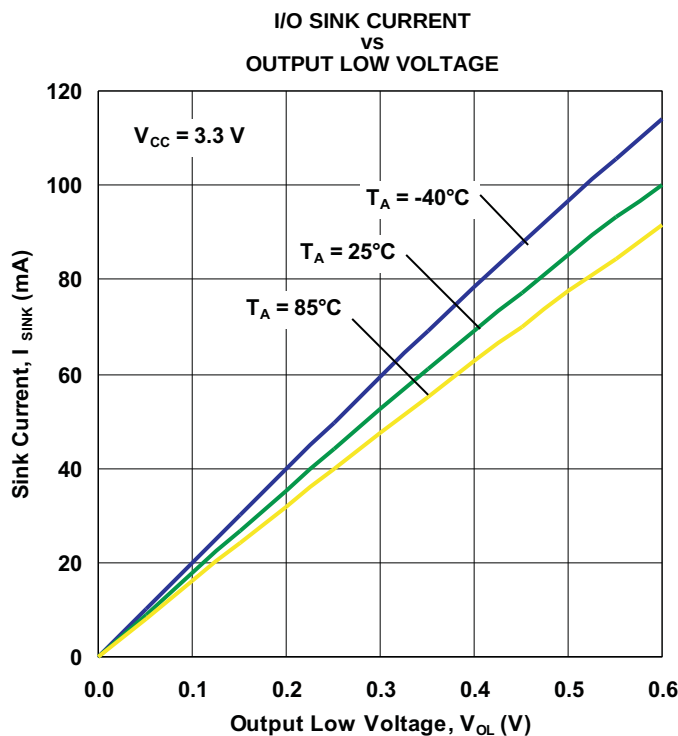
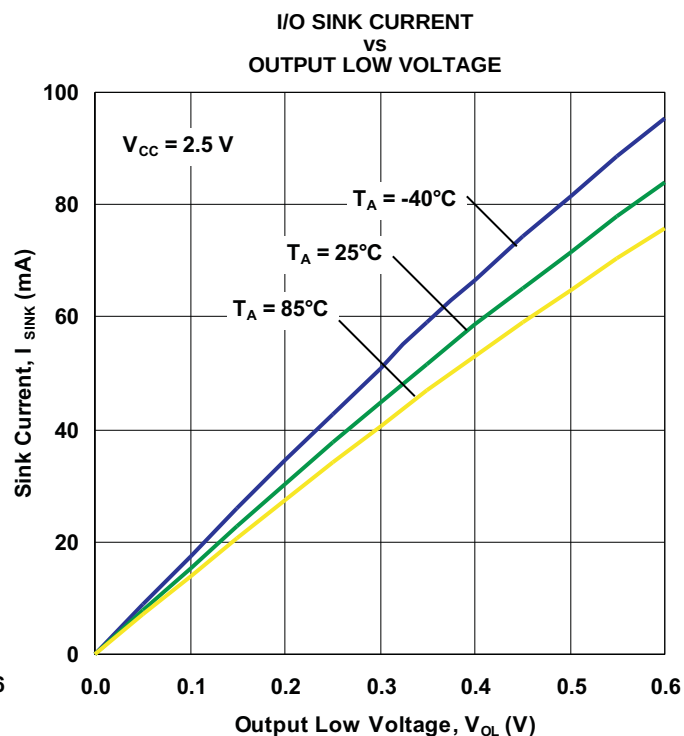
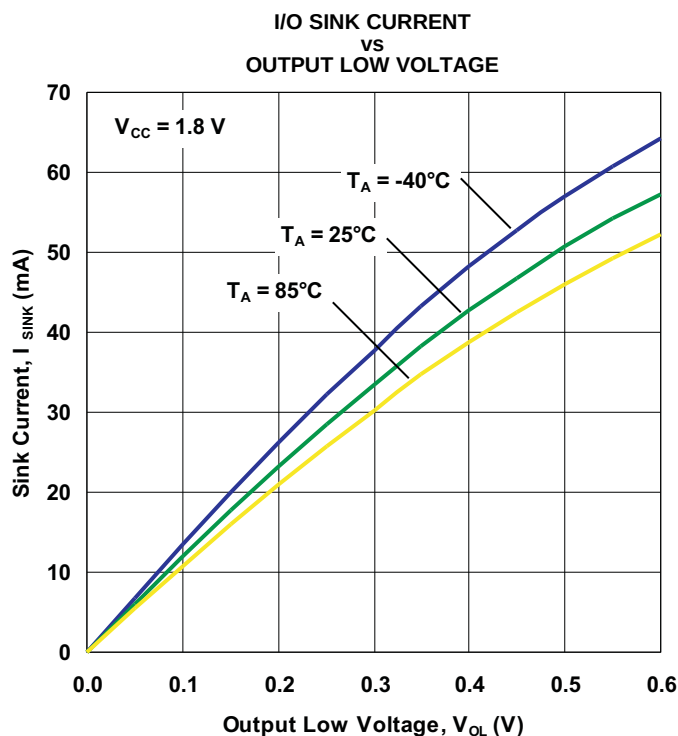
$T_A = 25^\circ\text{C}$  (unless otherwise noted)





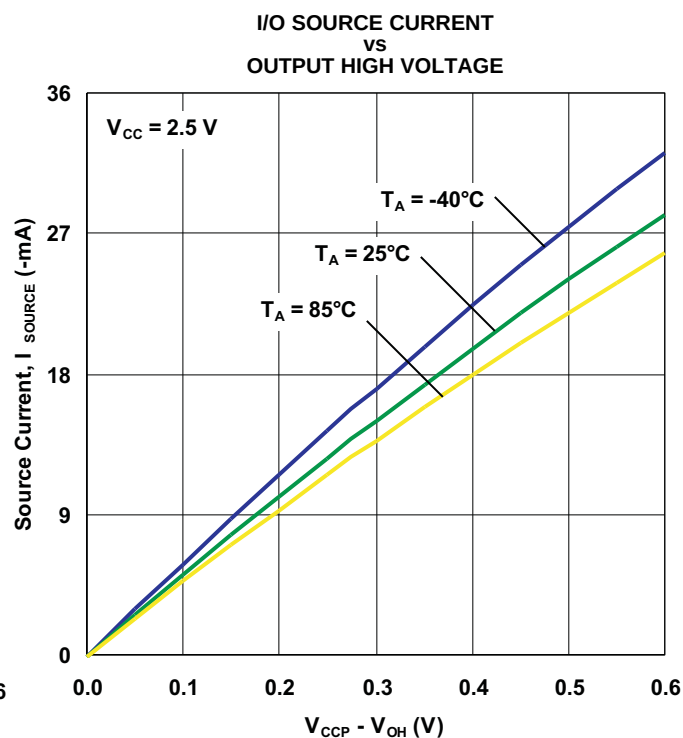
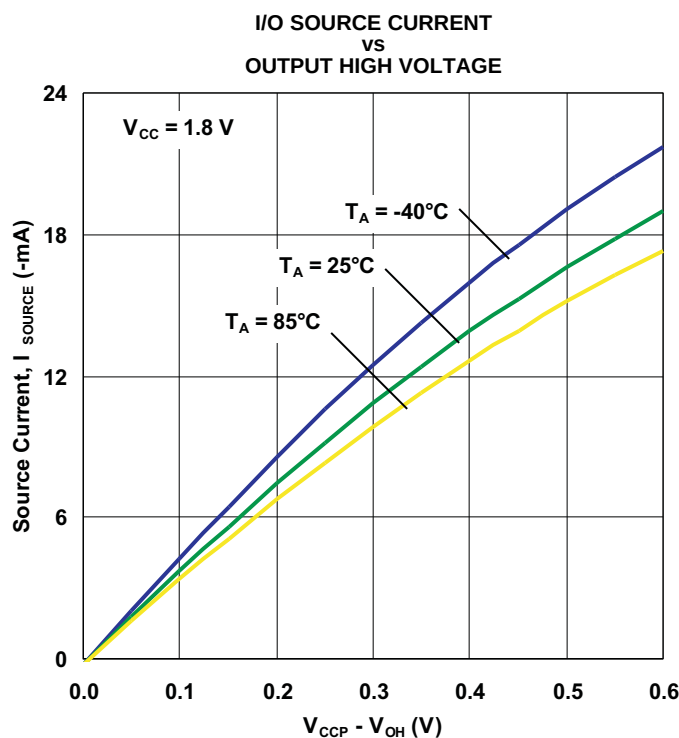
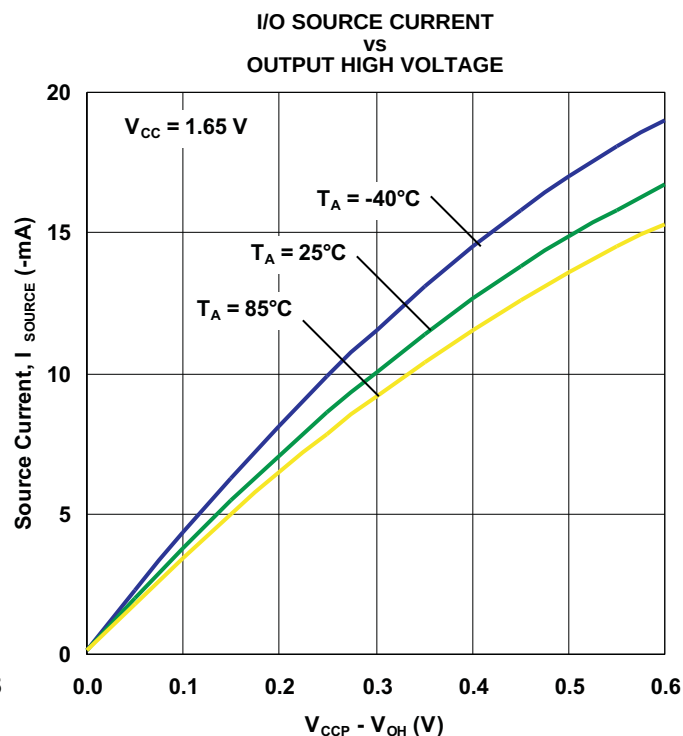
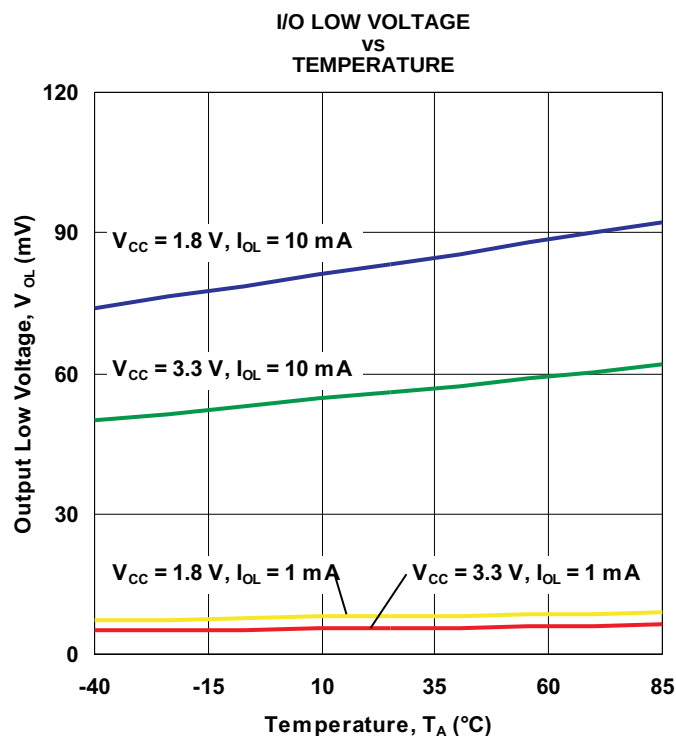
## TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)



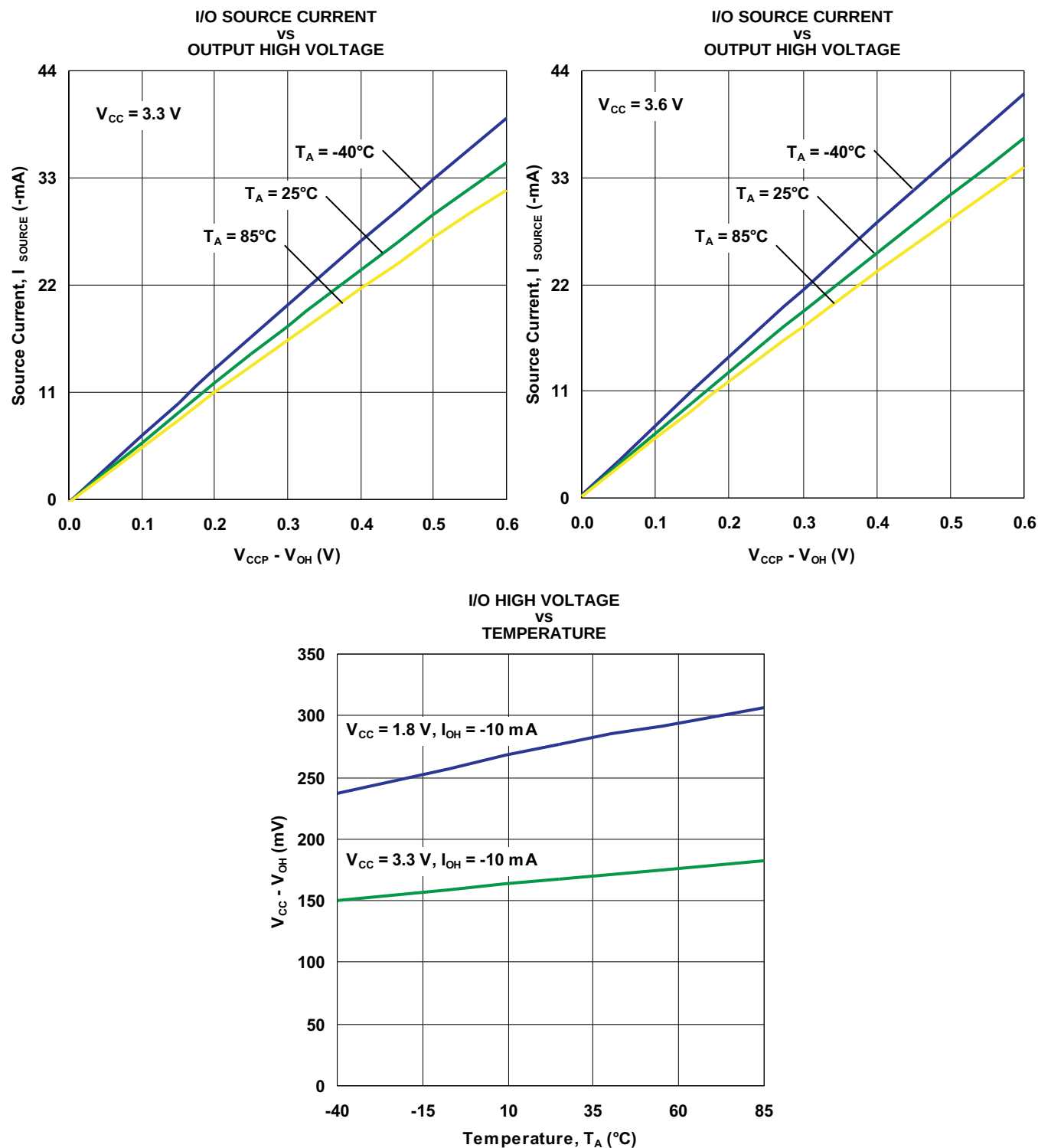
## TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

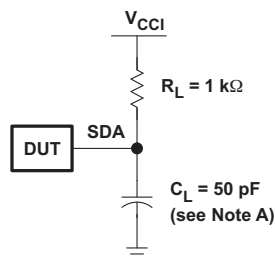


## TYPICAL CHARACTERISTICS (continued)

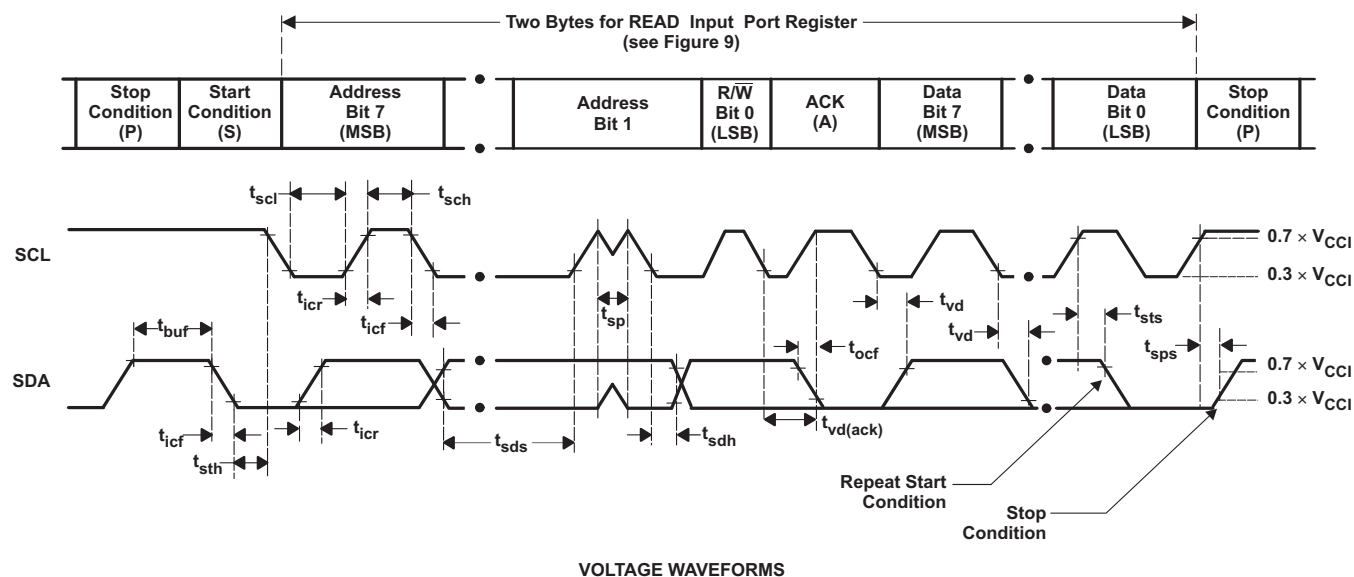
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



## PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



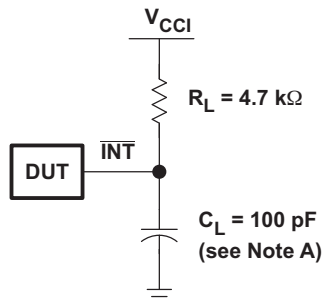
VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION              |
|------|--------------------------|
| 1    | I <sup>2</sup> C address |
| 2    | Input register port data |

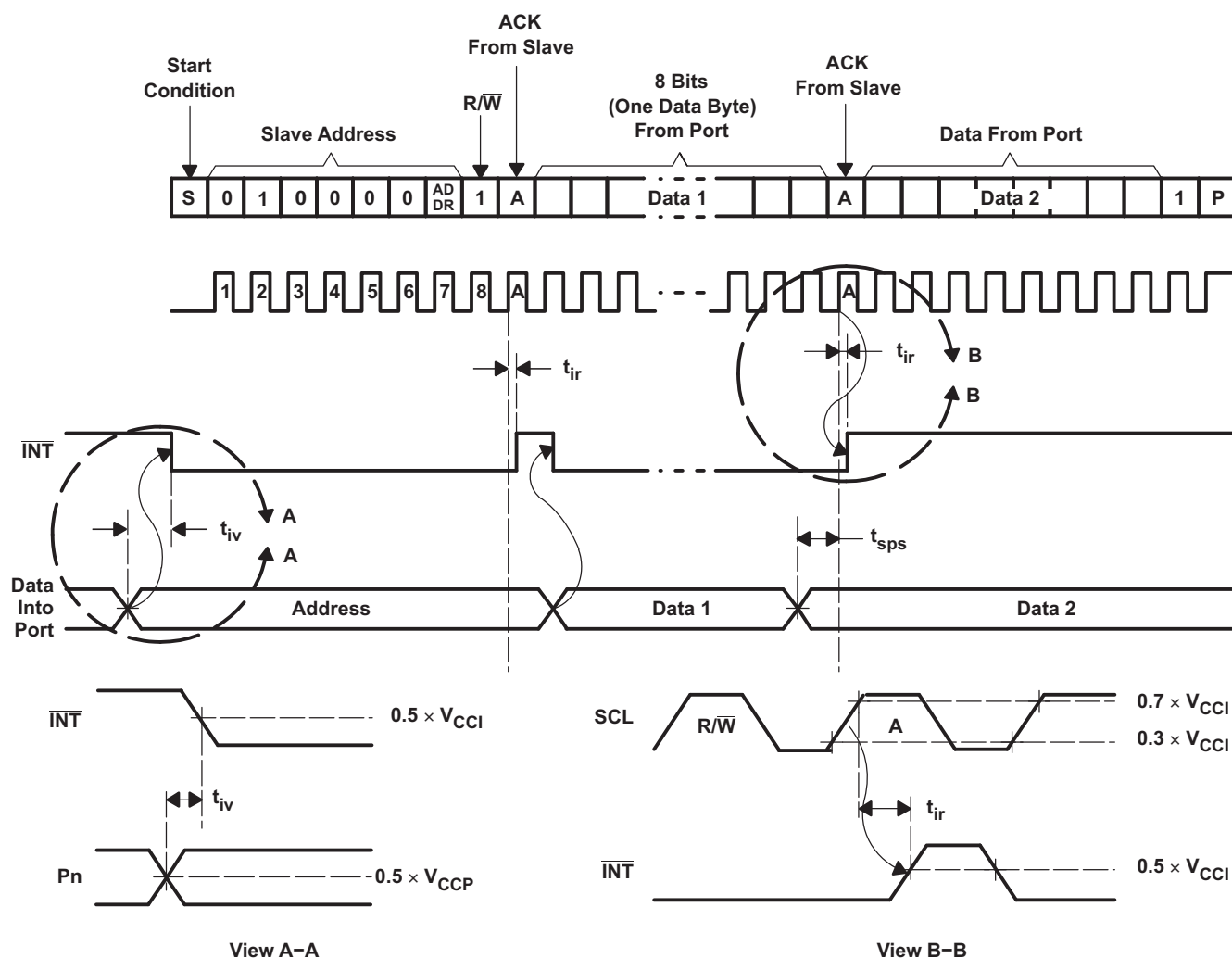
- A.  $C_L$  includes probe and jig capacitance.  $t_{ocf}$  is measured with  $C_L$  of 10 pF or 400 pF.
- B. All inputs are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r/t_f \leq 30\text{ ns}$ .
- C. All parameters and waveforms are not applicable to all devices.

**Figure 13. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)



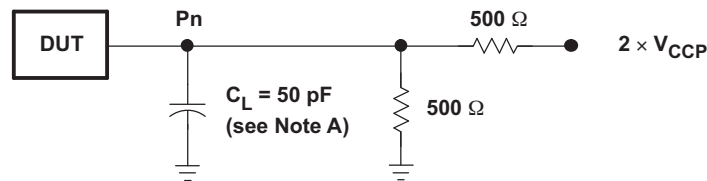
### INTERRUPT LOAD CONFIGURATION



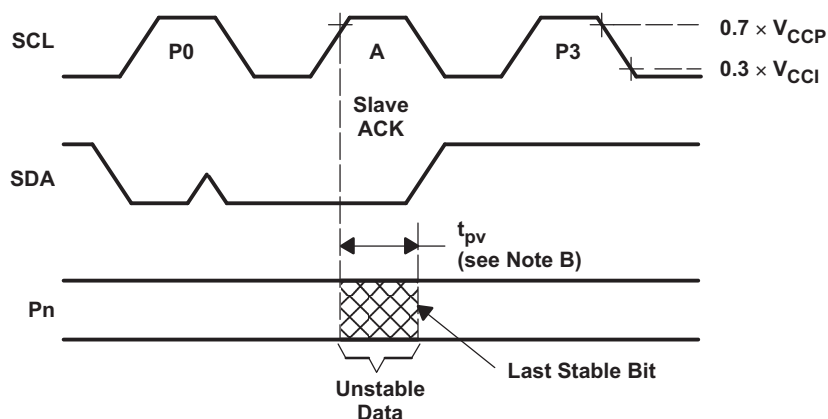
- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $\text{PRR} \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30 \text{ ns}$ .
- C. All parameters and waveforms are not applicable to all devices.

**Figure 14. Interrupt Load Circuit and Voltage Waveforms**

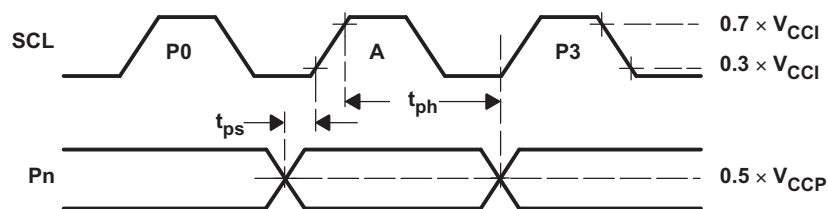
## PARAMETER MEASUREMENT INFORMATION (continued)



**P-PORT LOAD CONFIGURATION**



**WRITE MODE ( $R/\overline{W} = 0$ )**

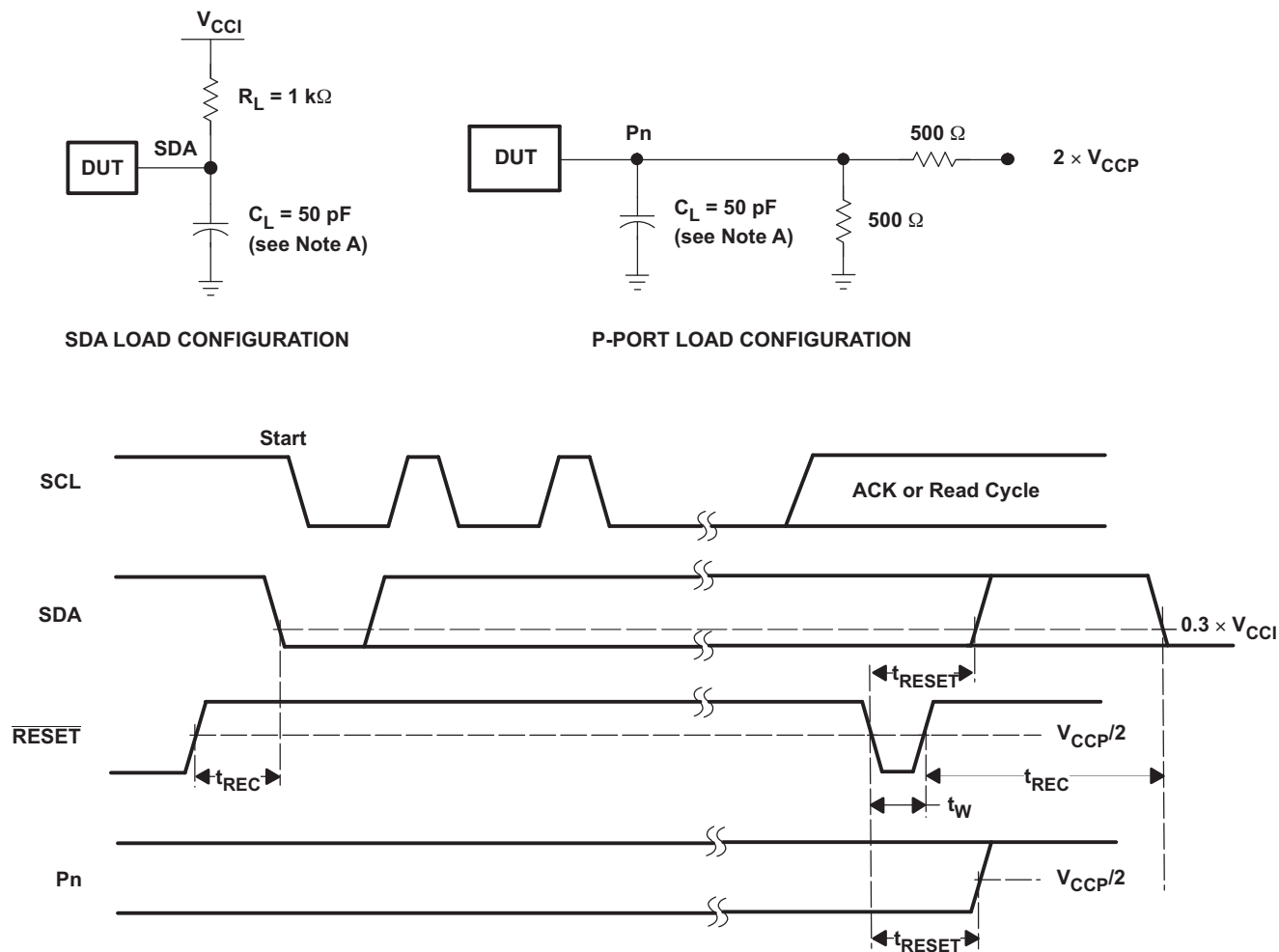


**READ MODE ( $R/\overline{W} = 1$ )**

- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 15. P Port Load Circuit and Timing Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)



- $C_L$  includes probe and jig capacitance.
- All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- The outputs are measured one at a time, with one transition per measurement.
- I/Os are configured as inputs.
- All parameters and waveforms are not applicable to all devices.

**Figure 16. Reset Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TCA8418RTWR      | ACTIVE                | QFN          | RTW             | 24   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

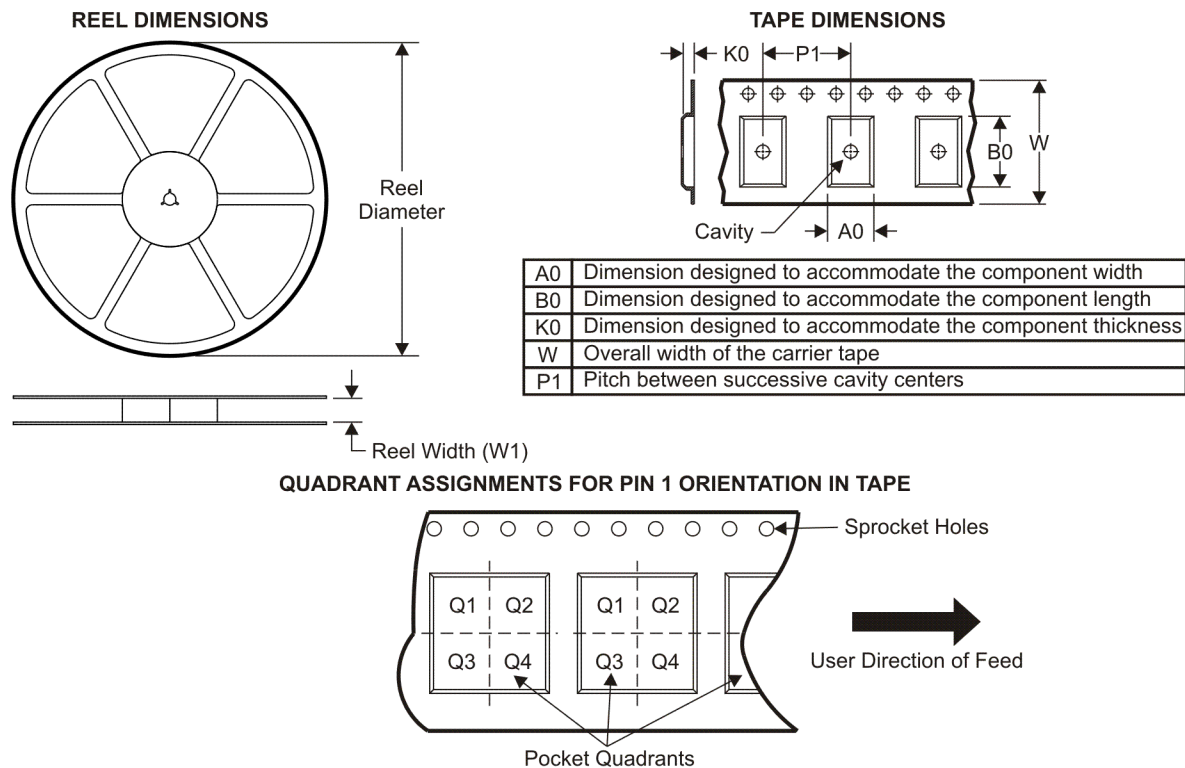
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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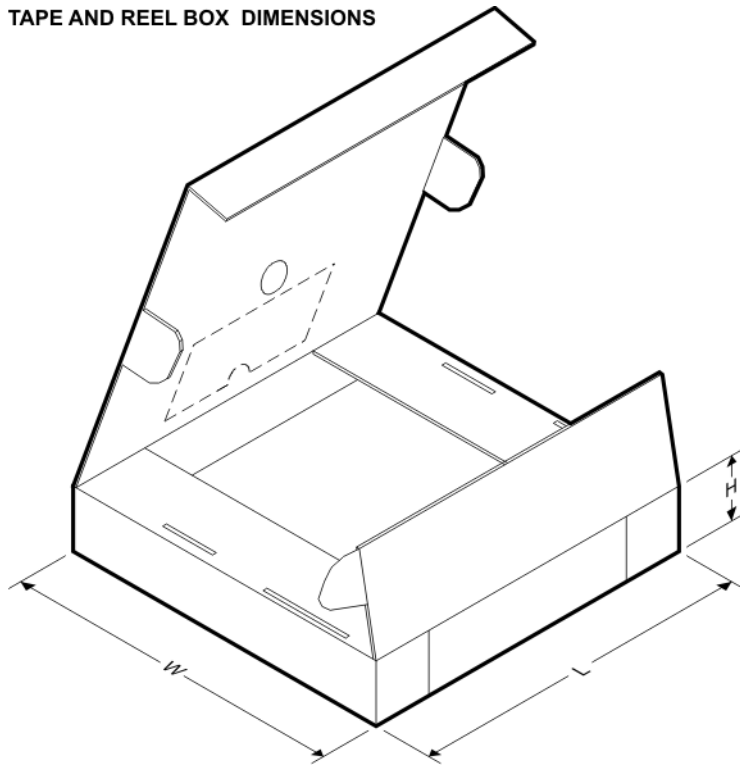


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TCA8418RTWR | QFN          | RTW             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

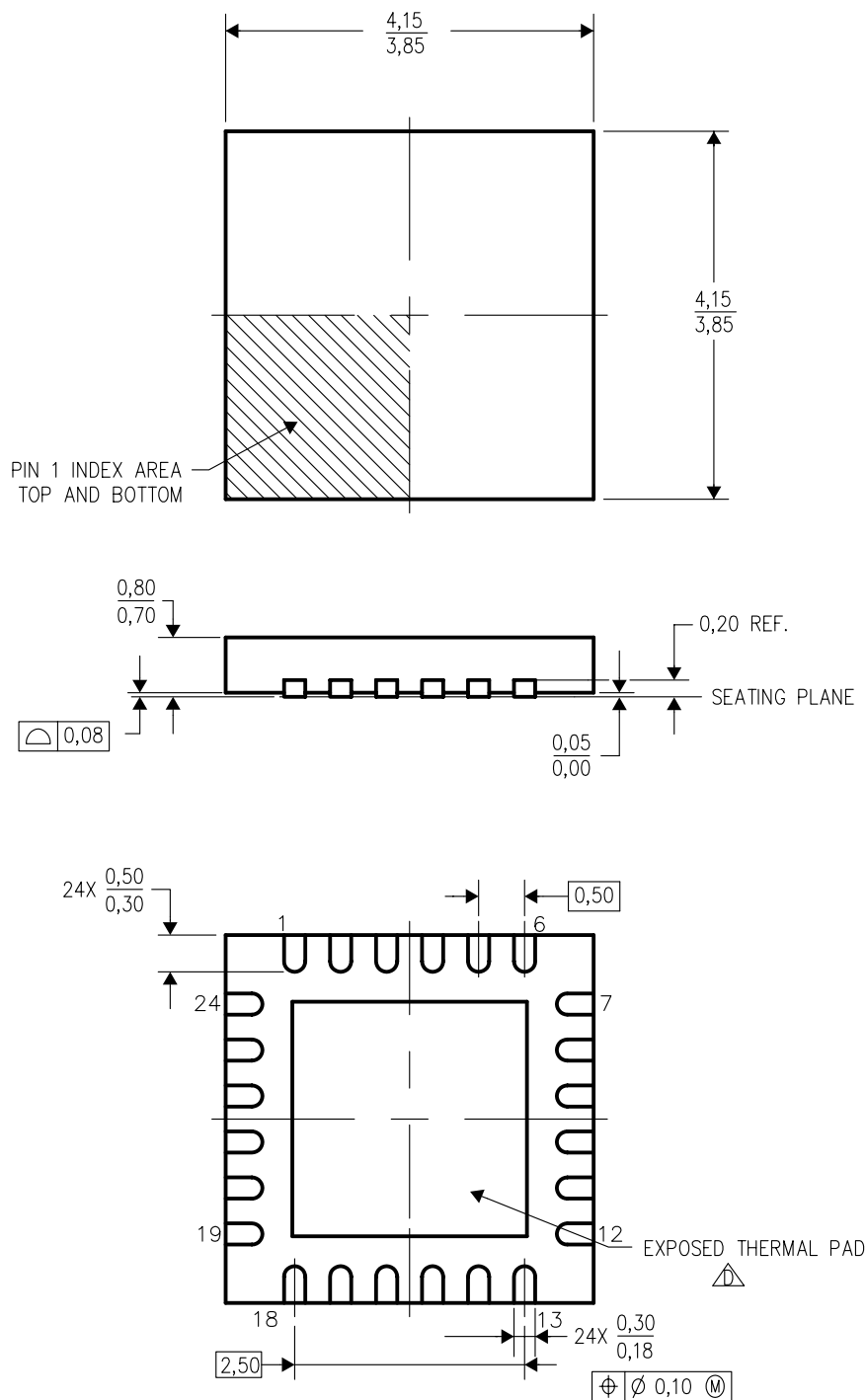


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TCA8418RTWR | QFN          | RTW             | 24   | 3000 | 346.0       | 346.0      | 29.0        |

RTW (S-PQFP-N24)

PLASTIC QUAD FLATPACK



4206244/A 07/04

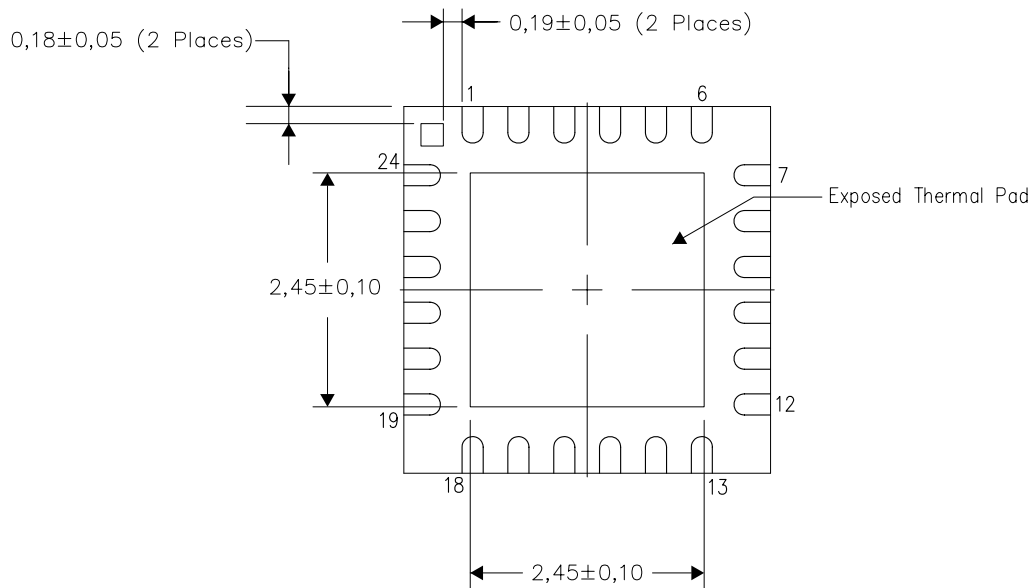
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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