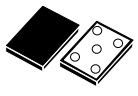
LD3985 SERIES

ULTRA LOW DROP-LOW NOISE BICMOS VOLTAGE REGULATORS LOW ESR CAPACITORS COMPATIBLE

- INPUT VOLTAGE FROM 2.5V TO 6V
- STABLE WITH LOW ESR CERAMIC CAPACITORS
- ULTRA LOW DROPOUT VOLTAGE (100mV TYP. AT 150mA LOAD, 0.4mV TYP. AT 1mA LOAD)
- VERY LOW QUIESCENT CURRENT (85µA TYP. AT NO LOAD, 170µA TYP. AT 150mA LOAD; MAX 1.5µA IN OFF MODE)
- GUARANTEED OUTPUT CURRENT UP TO 150mA
- WIDE RANGE OF OUTPUT VOLTAGE: 1.2V; 1.22V; 1.25V; 1.35V; 1.5V; 1.8V; 2V; 2.1V; 2.2V; 2.4V; 2.5V; 2.6V; 2.7V; 2.8V; 2.85V; 2.9V; 3V; 3.1V; 3.2V; 3.3V; 4.7V; 5V
- FAST TURN-ON TIME: TYP. 200µs [C_O=1µF, C_{BYP}= 10nF AND I_O=1mA]
- LOGIC-CONTROLLED ELECTRONIC SHUTDOWN
- INTERNAL CURRENT AND THERMAL LIMIT
- OUTPUT LOW NOISE VOLTAGE 30µVRMS OVER 10Hz to 100KHz
- S.V.R. OF 60dB AT 1KHz, 50dB AT 10KHz
- TEMPERATURE RANGE: -40°C TO 125°C



Flip-Chip (1.57x1.22)

SOT23-5L

TSOT23-5L

DESCRIPTION

The LD3985 provides up to 150mA, from 2.5V to 6V input voltage.

The ultra low drop-voltage, low quiescent current and low noise make it suitable for low power applications and in battery powered systems. Regulator ground current increases only slightly in dropout, further prolonging the battery life. Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10KHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits. Shutdown Logic Control function is available, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The LD3985 is designed to work with low ESR ceramic capacitors. Typical applications are in mobile phone and similar battery powered wireless systems.

Figure 1: Schematic Diagram

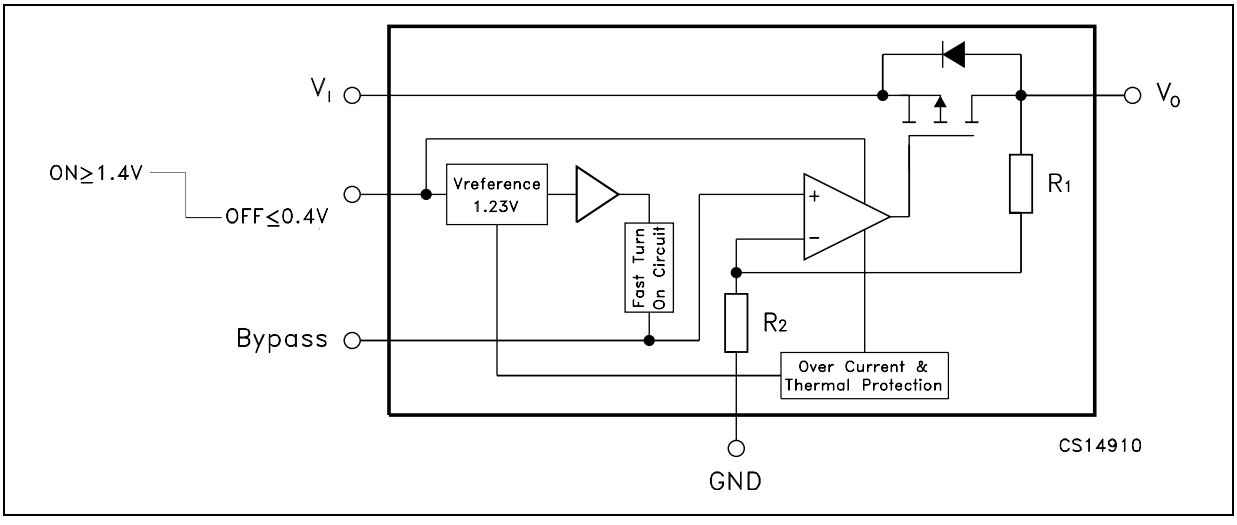


Table 1: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	-0.3 to 6 (*)	V
V_O	DC Output Voltage	-0.3 to V_I+0.3	V
V_{INH}	INHIBIT Input Voltage	-0.3 to V_I+0.3	V
I_O	Output Current	Internally limited	
P_D	Power Dissipation	Internally limited	
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{OP}	Operating Junction Temperature Range	-40 to 125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) The input pin is able to withstand non repetitive spike of 6.5V for 200ms.

Table 2: Thermal Data

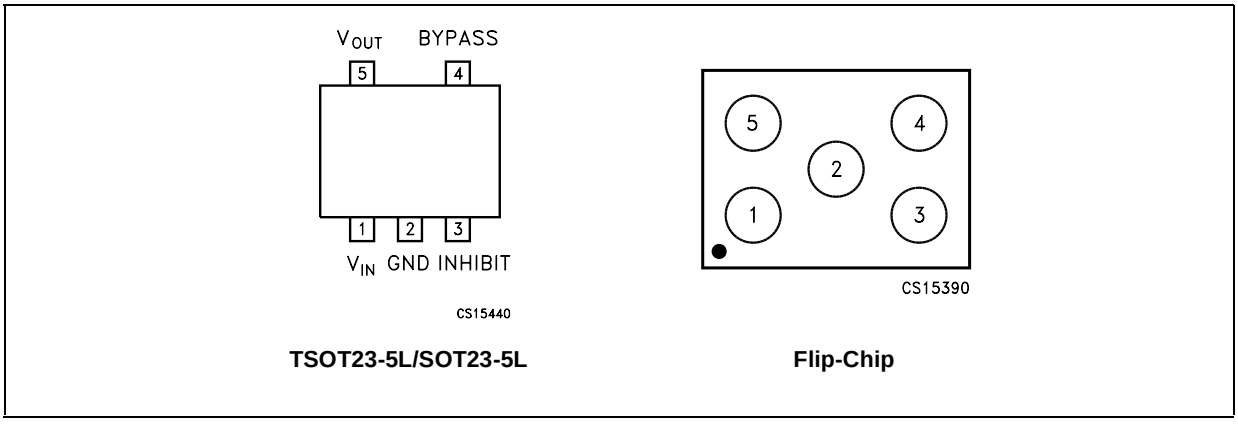
Symbol	Parameter	SOT23-5L/ TSOT23-5L	Flip-Chip	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	81		°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	255	170	°C/W

Table 3: Order Codes

SOT23-5L	TSOT23-5L	Flip-Chip	OUTPUT VOLTAGES
LD3985M12R (*)	LD3985G12R (*)	LD3985J12R (*)	1.20 V
LD3985M122R	LD3985G122R (*)	LD3985J122R	1.22 V
LD3985M125R (*)	LD3985G125R (*)	LD3985J125R	1.25 V
LD3985M135R (*)	LD3985G135R (*)	LD3985J135R	1.35 V
LD3985M15R	LD3985G15R (*)	LD3985J15R (*)	1.5 V
LD3985M18R	LD3985G18R	LD3985J18R	1.8 V
LD3985M20R (*)	LD3985G20R (*)	LD3985J20R (*)	2.0 V
LD3985M21R (*)	LD3985G21R (*)	LD3985J21R (*)	2.1 V
LD3985M22R (*)	LD3985G22R (*)	LD3985J22R (*)	2.2 V
LD3985M24R (*)	LD3985G24R (*)	LD3985J24R	2.4 V
LD3985M25R	LD3985G25R	LD3985J25R	2.5 V
LD3985M26R (*)	LD3985G26R (*)	LD3985J26R	2.6 V
LD3985M27R	LD3985G27R	LD3985J27R	2.7 V
LD3985M28R (*)	LD3985G28R (*)	LD3985J28R	2.8 V
LD3985M285R (*)	LD3985G285R (*)	LD3985J285R (*)	2.85 V
LD3985M29R	LD3985G29R	LD3985J29R	2.9 V
LD3985M30R (*)	LD3985G30R (*)	LD3985J30R	3.0 V
LD3985M31R (*)	LD3985G31R (*)	LD3985J31R	3.1 V
LD3985M32R (*)	LD3985G32R (*)	LD3985J32R (*)	3.2 V
LD3985M33R	LD3985G33R (*)	LD3985J33R	3.3 V
LD3985M44R (*)	LD3985G44R (*)	LD3985J44R (*)	4.4 V
LD3985M47R	LD3985G47R (*)	LD3985J47R	4.7 V
LD3985M48R (*)	LD3985G48R (*)	LD3985J48R	4.8 V
LD3985M49R (*)	LD3985G49R (*)	LD3985J49R (*)	4.9 V
LD3985M50R (*)	LD3985G50R (*)	LD3985J50R (*)	5.0 V

(*) Available on request.

Figure 2: Connection Diagram (top view for SOT and TSOT, top through view for Flip-Chip)



TSOT23-5L/SOT23-5L **Flip-Chip**

Table 4: Pin Description

Pin N° SOT23-5L/ TSOT23-5L	Pin N° Flip-Chip	Symbol	Name and Function
1	4	V_I	Input Voltage of the LDO
2	2	GND	Common Ground
3	1	V_{INH}	Inhibit Input Voltage: ON MODE when $V_{INH} \geq 1.2V$, OFF MODE when $V_{INH} \leq 0.4V$ (Do not leave floating, not internally pulled down/up)
4	5	BYPASS	Bypass Pin: Connect an external capacitor (usually 10nF) to minimize noise voltage
5	3	V_O	Output Voltage of the LDO

Figure 3: Typical Application Circuit

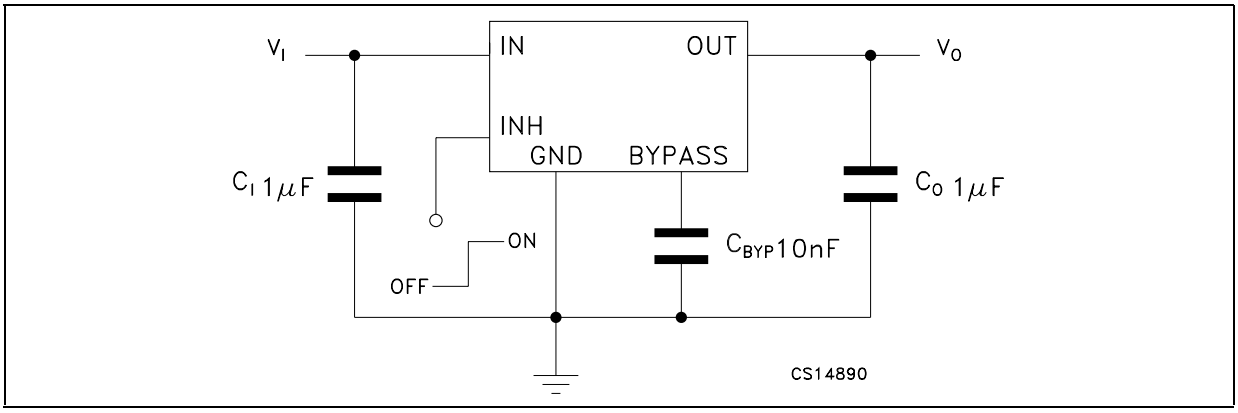


Table 5: Electrical Characteristics For LD3985 (T_j = 25°C, $V_I = V_{O(NOM)}$ +0.5V, C_I = 1µF, C_{BYP} = 10nF, I_O = 1mA, V_{INH} = 1.4V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Operating Input Voltage		2.5		6	V
V_O	Output Voltage < 2.5V	I_O = 1 mA	-50		50	mV
		T_J= -40 to 125°C	-75		75	
V_O	Output Voltage ≥ 2.5V	I_O = 1 mA	-2		2	% of $V_{O(NOM)}$
		T_J= -40 to 125°C	-3		3	
ΔV_O	Line Regulation (Note 1)	$V_I = V_{O(NOM)}$ + 0.5 to 6 V T_J= -40 to 125°C	-0.1		0.1	%/V
		V_O = 4.7 to 5V	-0.19		0.19	
ΔV_O	Load Regulation	I_O = 1 mA to 150mA V_O < 2.5V T_J= -40 to 125°C		0.002	0.008	%/mA
ΔV_O	Load Regulation	I_O = 1 mA to 150mA V_O ≥ 2.5V T_J= -40 to 125°C (for Flip-Chip)		0.0004	0.002	%/mA
		I_O = 1 mA to 150mA, T_J= -40 to 125°C (for SOT23-5L/TSOT23-5L), V_O ≥ 2.5V		0.0025	0.005	
ΔV_O	Output AC Line Regulation	$V_I = V_{O(NOM)}$ + 1 V, I_O = 150mA, $t_R = t_F$ = 30µs		1.5		mV_{PP}
I_Q	Quiescent Current ON MODE: V_{INH} = 1.2V	I_O = 0		85		µA
		I_O = 0 T_J= -40 to 125°C			150	
		I_O = 0 to 150mA		170		
		I_O = 0 to 150mA T_J= -40 to 125°C			250	
	OFF MODE: V_{INH} = 0.4V			0.003		
		T_J= -40 to 125°C			1.5	
V_{DROP}	Dropout Voltage (NOTE 1)	I_O = 1mA		0.4		mV
		I_O = 1mA T_J= -40 to 125°C			2	
		I_O = 50mA		20		
		I_O = 50mA T_J= -40 to 125°C			35	
		I_O = 100mA		45		
		I_O = 100mA T_J= -40 to 125°C			70	
		I_O = 150mA		60		
		I_O = 150mA T_J= -40 to 125°C			100	
I_{SC}	Short Circuit Current	R_L = 0		600		mA
SVR	Supply Voltage Rejection	$V_I = V_{O(NOM)}$+0.25V ± V_{RIPPLE} = 0.1V, I_O= 50mA $V_{O(NOM)}$ < 2.5V, V_I = 2.55V f = 1KHz		60		dB
		f = 10KHz		50		
$I_{O(PK)}$	Peak Output Current	$V_O \geq V_{O(NOM)}$ - 5%	300	550		mA
V_{INH}	Inhibit Input Logic Low	V_I = 2.5V to 6V T_J= -40 to 125°C			0.4	V
	Inhibit Input Logic High		1.2			
I_{INH}	Inhibit Input Current	V_{INH} = 0.4V V_I = 6V		±1		nA
eN	Output Noise Voltage	B_W = 10 Hz to 100 KHz C_O = 1 µF		30		μV_{RMS}
t_{ON}	Turn On Time (Note 4)	C_{BYP} = 10 nF		100	250	µs
T_{SHDN}	Thermal Shutdown	Note 5		160		°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_O	Output Capacitor	Capacitance (Note 6)	1		22	µF
		ESR	5		5000	mΩ

Note 1 – For $V_{O(NOM)} < 2V$, $V_I = 2.5V$
Note 2 – For $V_{O(NOM)} = 1.25V$, $V_I = 2.5V$
Note 3 – Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.
Note 4 – Turn-on time is time measured between the enable input just exceeding V_{INH} High Value and the output voltage just reaching 95% of its nominal value
Note 5 – Typical thermal protection hysteresis is 20°C
Note 6 - The minimum capacitor value is 1µF, anyway the LD3985 is still stable if the compensation capacitor has a 30% tolerance in all temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS (T_j = 25°C, $V_I = V_{O(NOM)}$ +0.5V, $C_I = C_O$ = 1µF, C_{BYP} = 10nF, I_O = 1mA, V_{INH} = 1.4V, unless otherwise specified)

Figure 4: Output Voltage vs Temperature

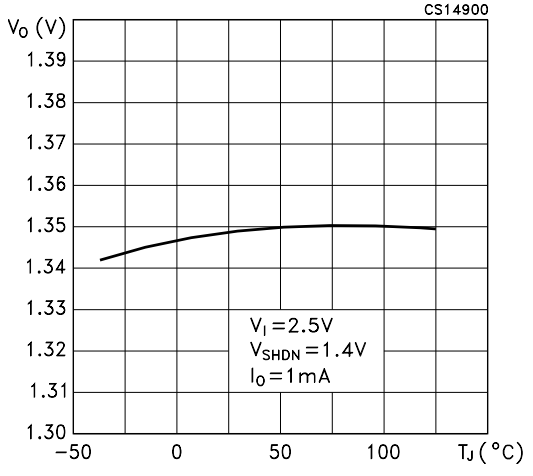


Figure 5: Output Voltage vs Temperature

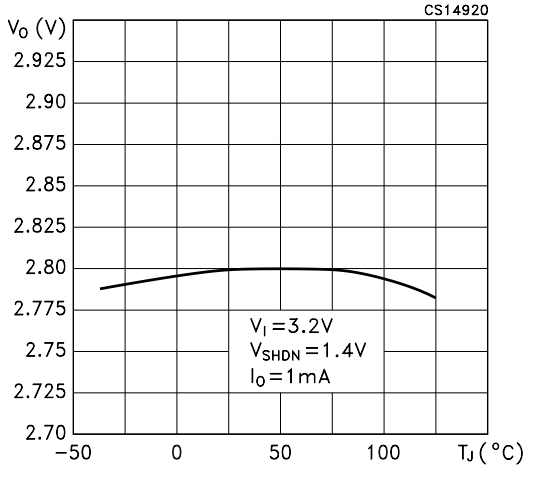


Figure 6: Output Voltage vs Temperature

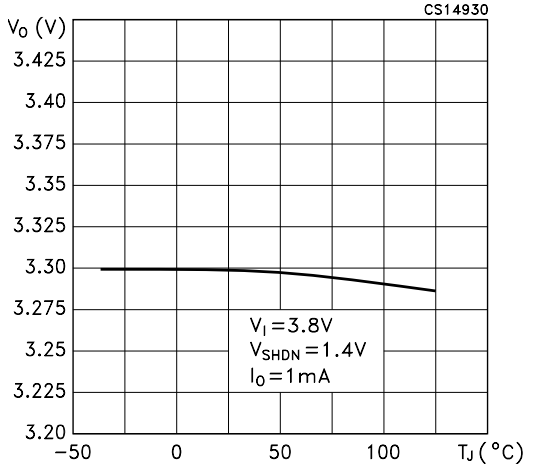


Figure 7: Shutdown Voltage vs Temperature

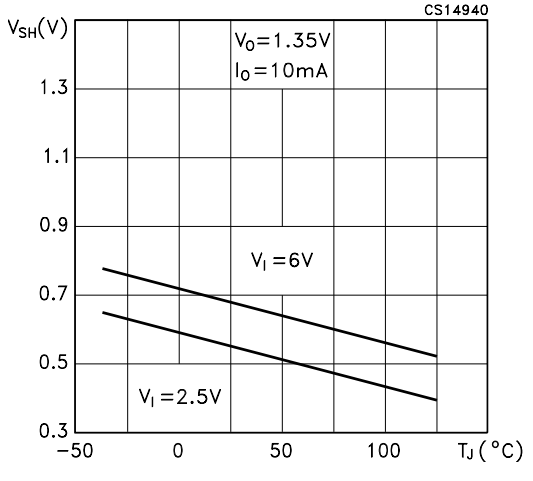


Figure 8: Shutdown Voltage vs Temperature

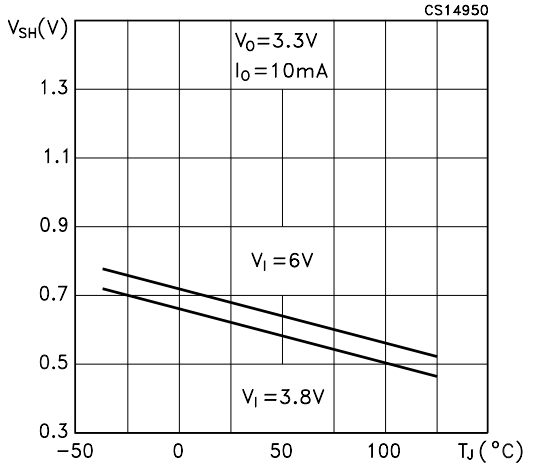


Figure 9: Line Regulation vs Temperature

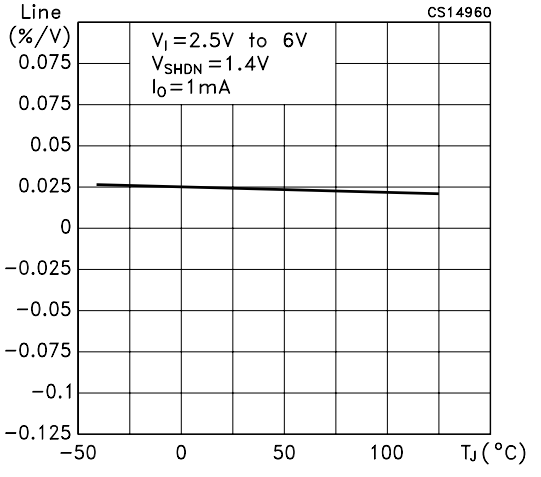


Figure 10: Line Regulation vs Temperature

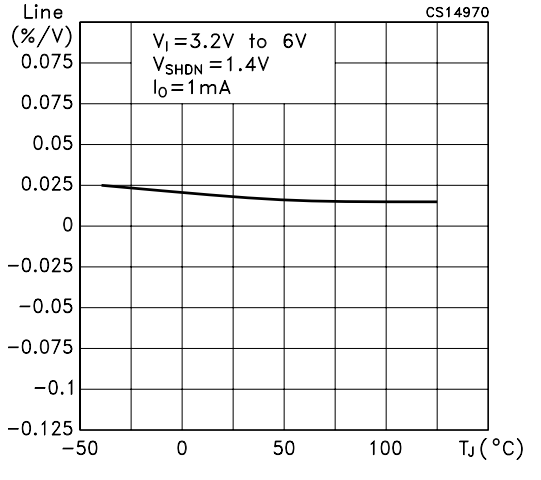


Figure 11: Line Regulation vs Temperature

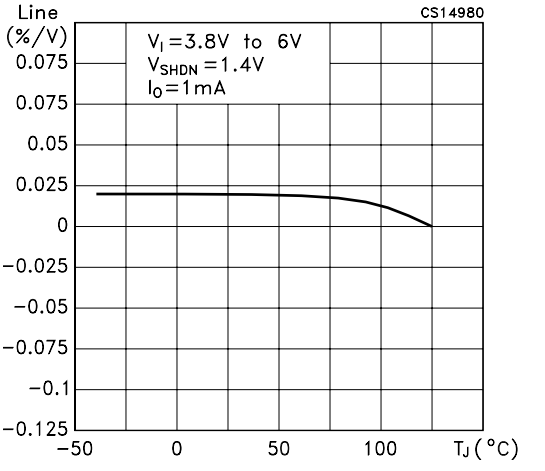


Figure 12: Load Regulation vs Temperature

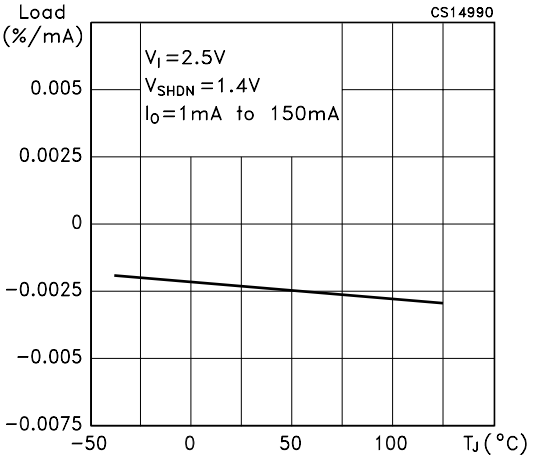


Figure 13: Load Regulation vs Temperature

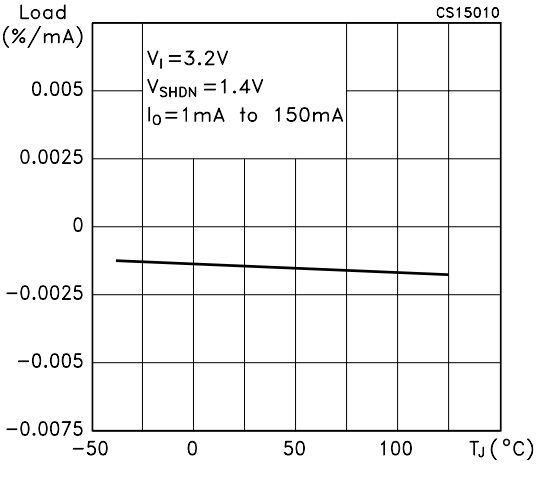


Figure 14: Load Regulation vs Temperature

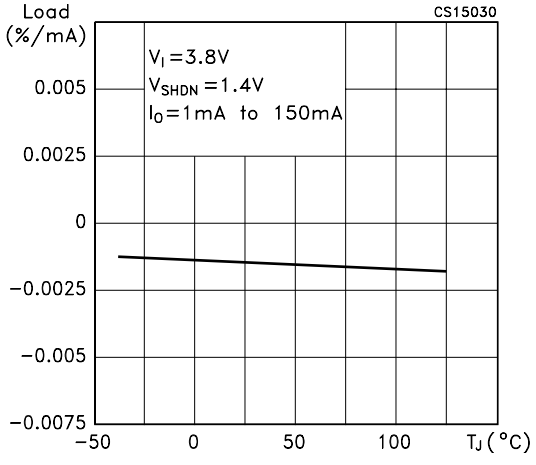


Figure 15: Quiescent Current vs Temperature

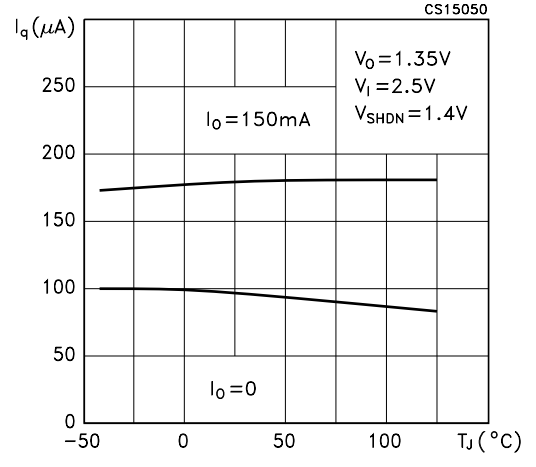


Figure 16: Quiescent Current vs Temperature

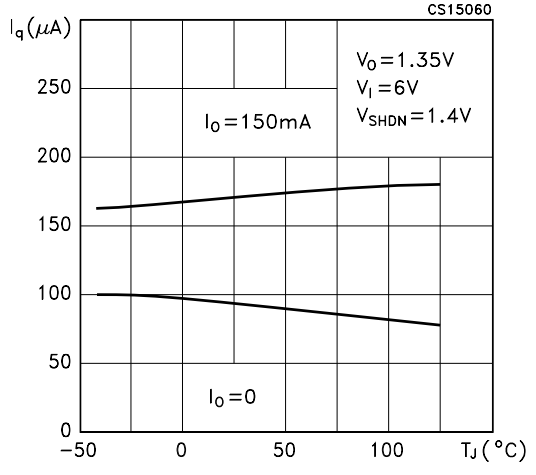


Figure 17: Quiescent Current vs Temperature

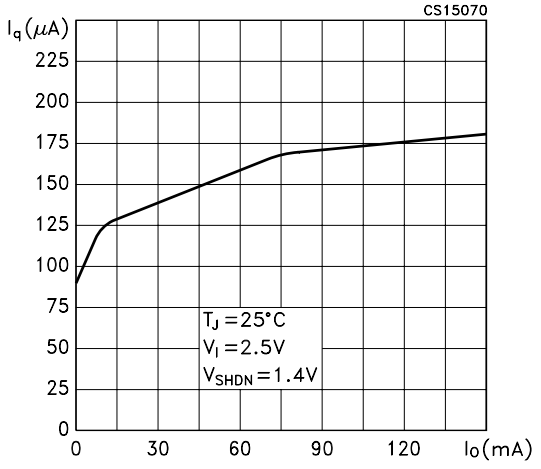


Figure 18: Supply Voltage Rejection vs Frequency

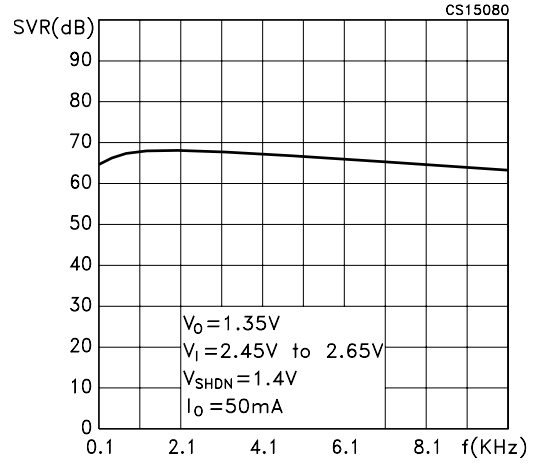
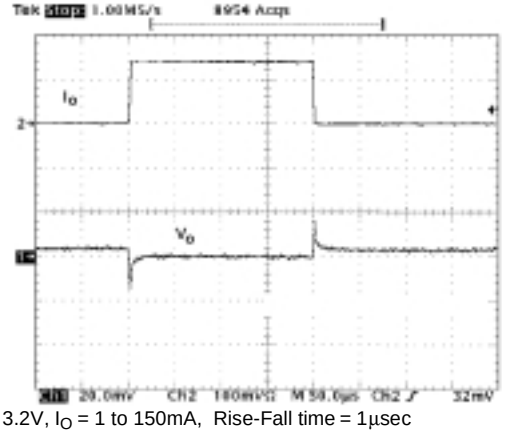
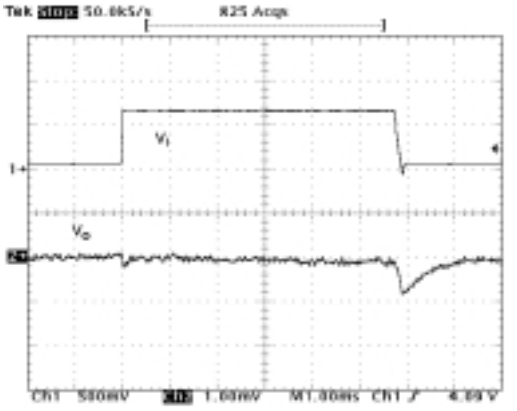


Figure 19: Load Transient Response



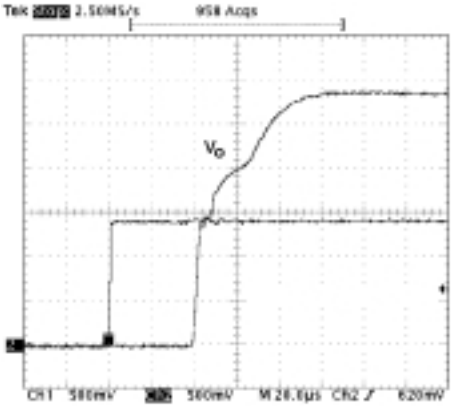
V_I = 3.2V, I_O = 1 to 150mA, Rise-Fall time = 1µsec

Figure 20: Line Transient Response



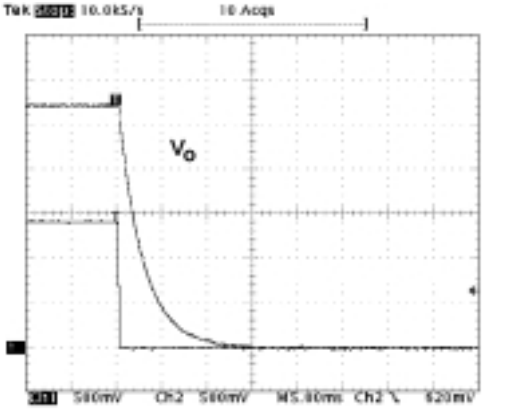
V_I = 3.8V to 4.4V, T_J = 25°C, I_O = 150mA, C_I = C_O = 1µF (X7R), C_{BYP} = 10nF, Rise-Fall time = 1µsec, V_O = 2.7V

Figure 21: START-UP



V_I = 3.3V, I_O = 1mA, C_I = C_O = 1µF (cer), C_{BYP} = 10nF, T_r = 20ns, V_O = 2.8V

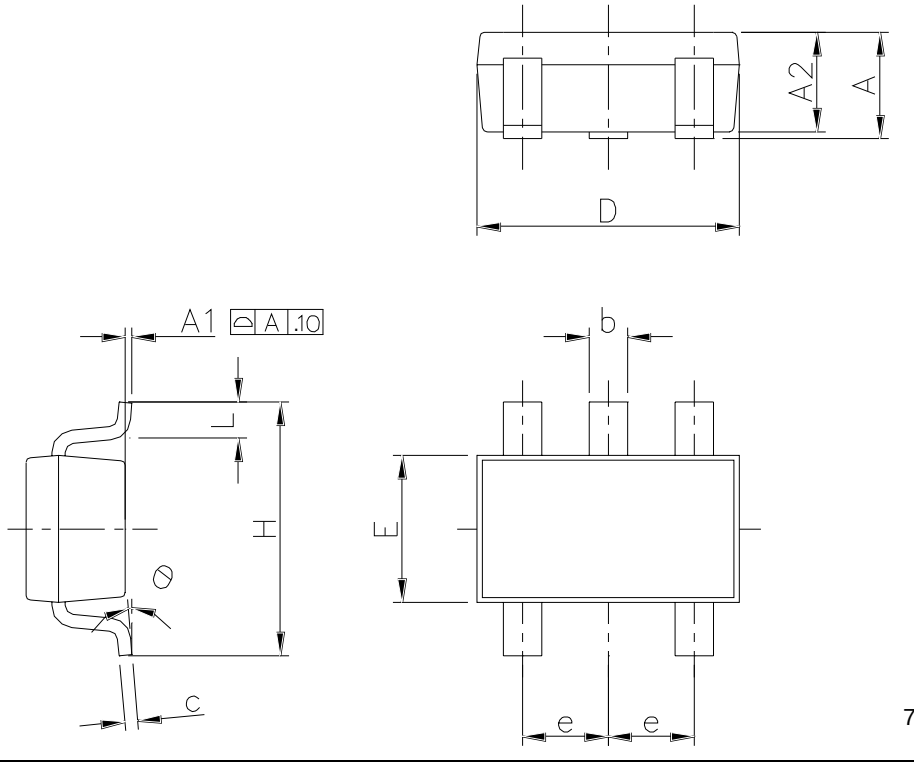
Figure 22: TURN-OFF



V_I = 3.3V, I_O = 1mA, C_I = C_O = 1µF (cer), C_{BYP} = 10nF, T_f = 20ns, V_O = 2.8V

SOT23-5L MECHANICAL DATA

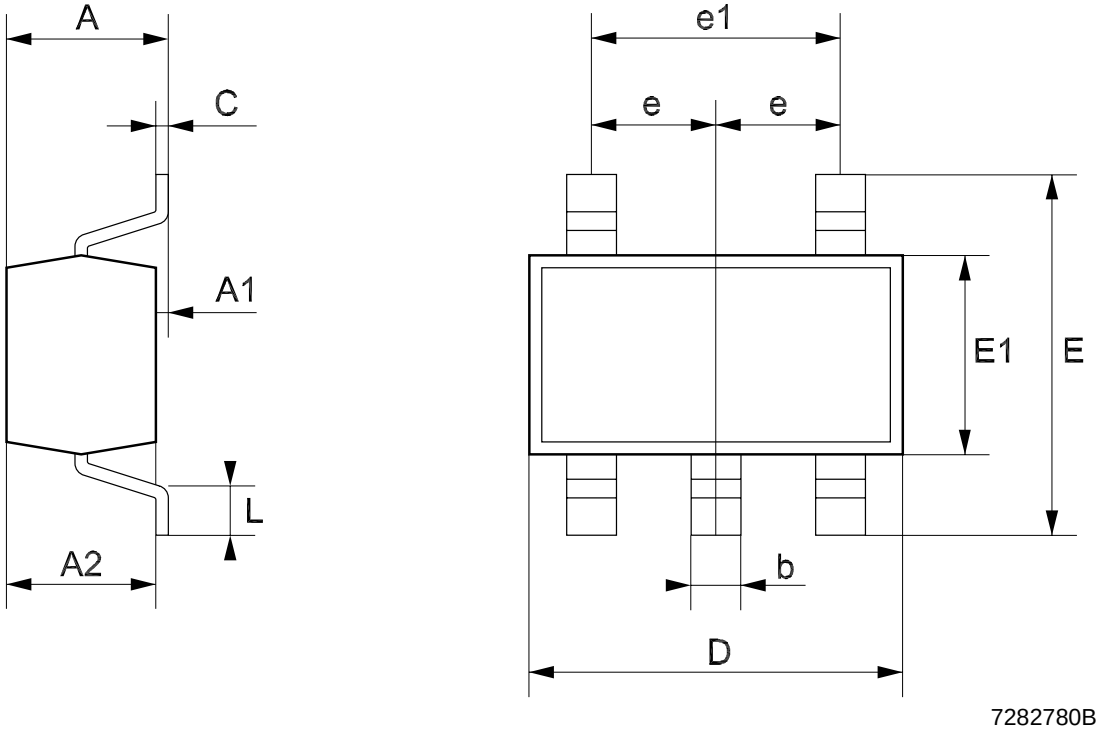
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



7049676C

TSOT23-5L MECHANICAL DATA

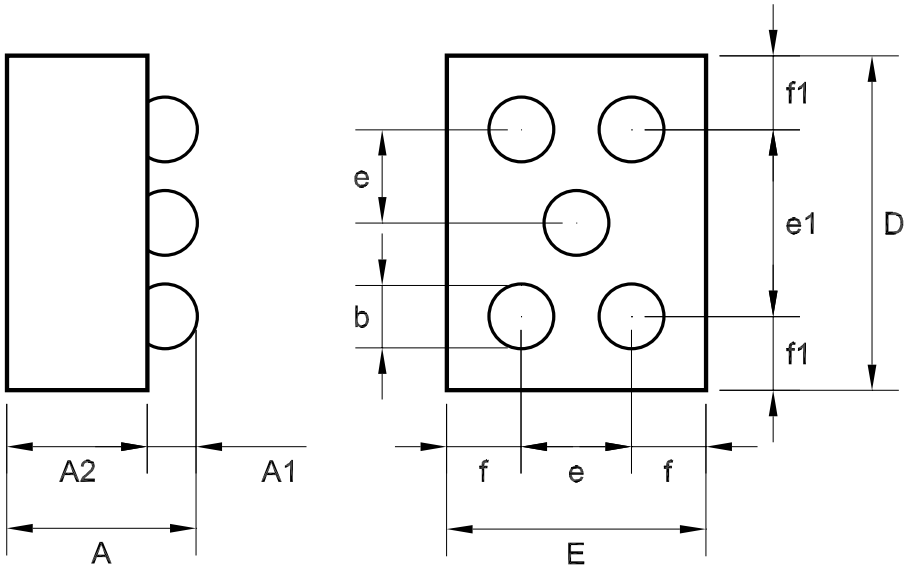
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			43.3
A1	0		0.1			3.9
A2	0.7		1.0	27.6		39.4
b	0.3		0.5	11.8		19.7
C	0.08		0.2	3.1		7.9
D		2.9			114.2	
E		2.8			110.2	
E1		1.6			63.0	
e		0.95			37.4	
e1		1.9			74.8	
L	0.3		0.6	11.8		23.6



7282780B

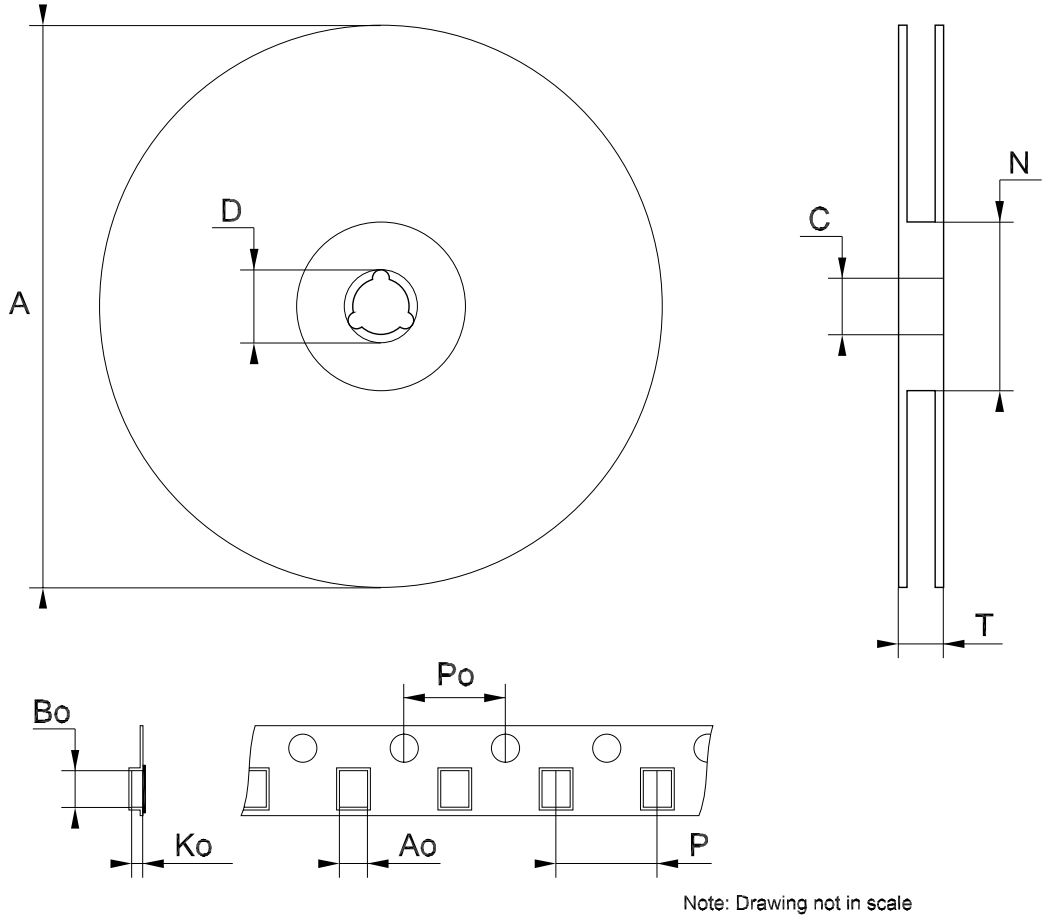
Flip-Chip5 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.835	0.9	0.965	32.874	35.433	37.992
A1	0.21	0.25	0.29	8.268	9.843	11.417
A2	0.625	0.65	0.675	24.606	25.591	26.575
b	0.265	0.315	0.365	10.433	12.402	14.370
D	1.510	1.540	1.570	59.449	60.630	61.811
E	1.16	1.19	1.22	45.669	46.850	48.031
e	0.45	0.5	0.55	17.717	19.685	21.654
e1	0.816	0.866	0.916	32.126	34.094	36.063
f		0.345			13.583	
f1		0.337			13.268	



Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.0.58
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Note: Drawing not in scale

Table 6: Revision History

Date	Revision	Description of Changes
07-May-2004	6	Part Number Status Changed on Table 3.
05-Oct-2004	7	t_{ON} values are Changed on Table 5.
27-Oct-2004	8	Order Codes changed - Table 3.

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